Features

- Full-duplex Operation Mode without Duplex Frequency Offset to Prevent the Relay Attack against Passive Entry Go (PEG) Systems
- High FSK Sensitivity: –105.5 dBm at 20 Kbit/s/–109 dBm at 2.4 Kbit/s (433.92 MHz)
- High ASK Sensitivity: –111.5 dBm at 10 Kbit/s/–116 dBm at 2.4 Kbit/s (100% ASK, Carrier Level 433.92 MHz)
- Low Supply Current: 10.5 mA in RX and TX Mode (3V/TX with 5 dBm/433.92 MHz)
- Data Rate 1 to 20 Kbit/s Manchester FSK, 1 to 10 Kbit/s Manchester ASK
- ASK/FSK Receiver Uses a Low IF Architecture with High Selectivity, Blocking and Low Intermodulation (Typical 3 dB Blocking 55.5 dBC at ±750 kHz/60.5 dBC at ±1.5 MHz and 67 dBC at ±10 MHz, System I1dBCP = –30 dBm/System IIP3 = –20 dBm)
- Wide Bandwidth AGC to Handle Large Outband Blockers above the System I1dBCP
- 226 kHz IF (Intermediate Frequency) with 30 dB Image Rejection and 220 kHz System Bandwidth to Support TPM Transmitters using ATA5756/ATA5757 Transmitters with Standard Crystals
- Transmitter Uses Closed Loop FSK Modulation with Fractional-N Synthesizer with High PLL Bandwidth and an Excellent Isolation between PLL and PA
- Tolerances of XTAL Compensated by Fractional-N Synthesizer with 800 Hz RF Resolution
- Integrated RX/TX-Switch, Single-ended RF Input and Output
- RSSI (Received Signal Strength Indicator)
- Communication to Microcontroller with SPI Interface Working at 500 kBit/s Maximum
- Configurable Self Polling and RX/TX Protocol Handling with FIFO-RAM Buffering of Received and Transmitted Data
- 1 Push Button Input and 1 Wake-up Input are Active in Power-down Mode
- Integrated XTAL Capacitors
- PA Efficiency: up to 38% (433.92 MHz/10 dBm/3V)
- Low In-band Sensitivity Change of Typically ±2.0 dB within ±75 kHz Center Frequency Change in the Complete Temperature and Supply Voltage Range
- Fully Integrated PLL with Low Phase Noise VCO, PLL Loop Filter and full support of multi-channel operation with arbitrary Channel distance due to Fractional-N Synthesizer
- Sophisticated Threshold Control and Quasi-peak Detector Circuit in the Data Slicer
- 433.92 MHz, 868.3 MHz and 315 MHz without External VCO and PLL Components
- Efficient XTO Start-up Circuit (> –1.5 kΩ Worst Case Start Impedance)
- Changing of Modulation Type ASK/FSK and Data Rate without Component Changes to Allow Different Modulation Schemes in TPM and RKE
- Minimal External Circuitry Requirements for Complete System Solution
- Adjustable Output Power: 0 to 10 dBm Adjusted and Stabilized with External Resistor, Programmable Output Power with 0.5dB Steps with Internal Resistor
- Clock and Interrupt Generation for Microcontroller
- ESD Protection at all Pins (±2.5 kV HBM, ±200V MM, ±500V FCDM)
- Supply Voltage Range: 2.15V to 3.6V or 4.4V to 5.25V
- Typical Power-down Current < 10 nA
- Temperature Range: –40°C to +105°C
- Small 7 mm × 7 mm QFN48 Package

UHF ASK/FSK Transceiver

ATA5823
ATA5824

4829D–RKE–06/06

Applications

- **Automotive Keyless Entry and Passive Entry Go (Handsfree Car Access)**
- **Tire Pressure Monitoring Systems**
- **Remote Control Systems**
- **Alarm and Telemetering Systems**
- **Energy Metering**
- **Home Automation**

Benefits

- **No SAW Device Needed in Key Fob Designs to Meet Automotive Specifications**
- **Low System Cost Due to Very High System Integration Level**
- **Only One Crystal Needed in System**
- **Less Demanding Specification for the Microcontroller Due to Handling of Power-down Mode, Delivering of Clock and Complete Handling of Receive/Transmit Protocol and Polling**
- **Single-ended Design with High Isolation of PLL/VCO from PA and the Power Supply Allows a Loop Antenna in the Key Fob to Surround the Whole Application**
- **Prevention against Relay Attack with Full-duplex Operation Mode**
- **Integration of Tire Pressure Monitoring, Passive Entry and Remote Keyless Entry**

1. General Description

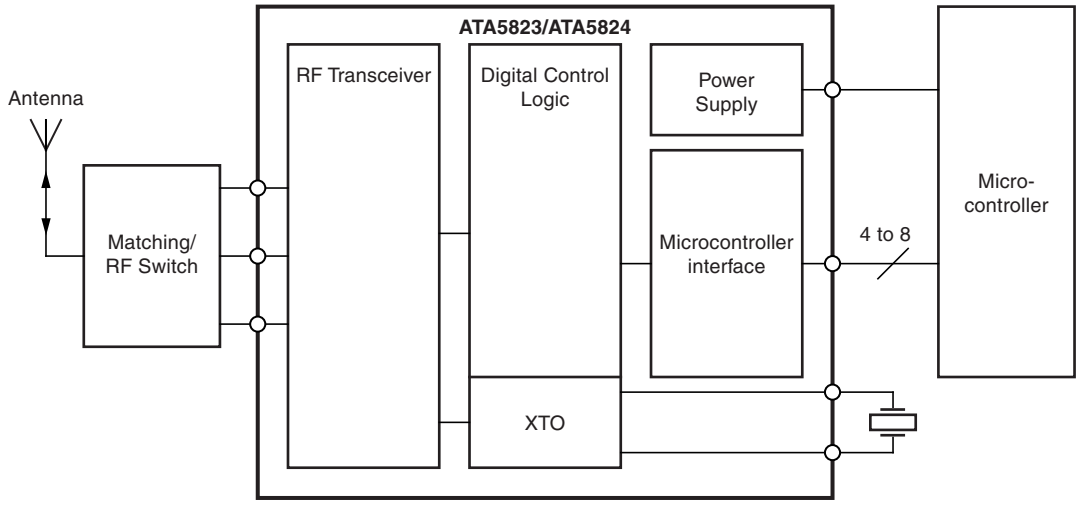
The ATA5823/ATA5824 is a highly integrated UHF ASK/FSK multi-channel half-duplex and full-duplex transceiver with low power consumption supplied in a small 7 mm × 7 mm QFN48 package. The receive part is built as a fully integrated low-IF receiver, whereas direct PLL modulation with the fractional-N synthesizer is used for FSK transmission and switching of the power amplifier for ASK transmission. The additional full-duplex mode makes relay attacks much more difficult, since the attacker has to receive and transmit signals on the same frequency at the same time.

The device supports data rates of 1 Kbit/s to 20 Kbit/s (FSK) and 1 Kbit/s to 10 Kbit/s (ASK) in Manchester, Bi-phase and other codes in transparent mode. The ATA5824 can be used in the 433 MHz to 435 MHz band and the 867 MHz to 870 MHz band, the ATA5823 in the 313 MHz to 316 MHz band. The very high system integration level results in few numbers of external components needed.

Due to its blocking and selectivity performance, together with a typical narrow-band key-fob loop antenna with 15 dB to 20 dB loss, a bulky blocking SAW is not needed in the key fob application. Additionally, the building blocks needed for a typical RKE and access control system on both sides, the base and the mobile stations, are fully integrated.

Its digital control logic with self polling and protocol generation provides a fast challenge response system without using a high-performance microcontroller. Therefore, the ATA5823/ATA5824 contains a FIFO buffer RAM and can compose and receive the physical messages themselves. This provides more time for the microcontroller to carry out other functions such as calculating crypto algorithms, composing the logical messages and controlling other devices. Due to that, a standard 4-/8-bit microcontroller without special periphery and clocked with the delivered CLK output of about 4.5 MHz is sufficient to control the communication link. This is especially valid for passive entry go and access control systems, where within less than 100 ms several communication responses with arbitration of the communication partner have to be handled. It is hence possible to design bi-directional RKE and passive entry go systems with a fast challenge response crypto function and prevention against relay attacks.

Figure 1-1. System Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN48

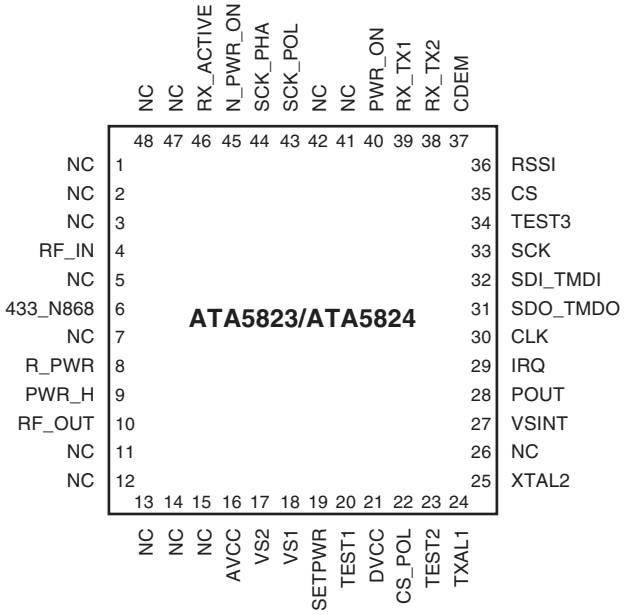


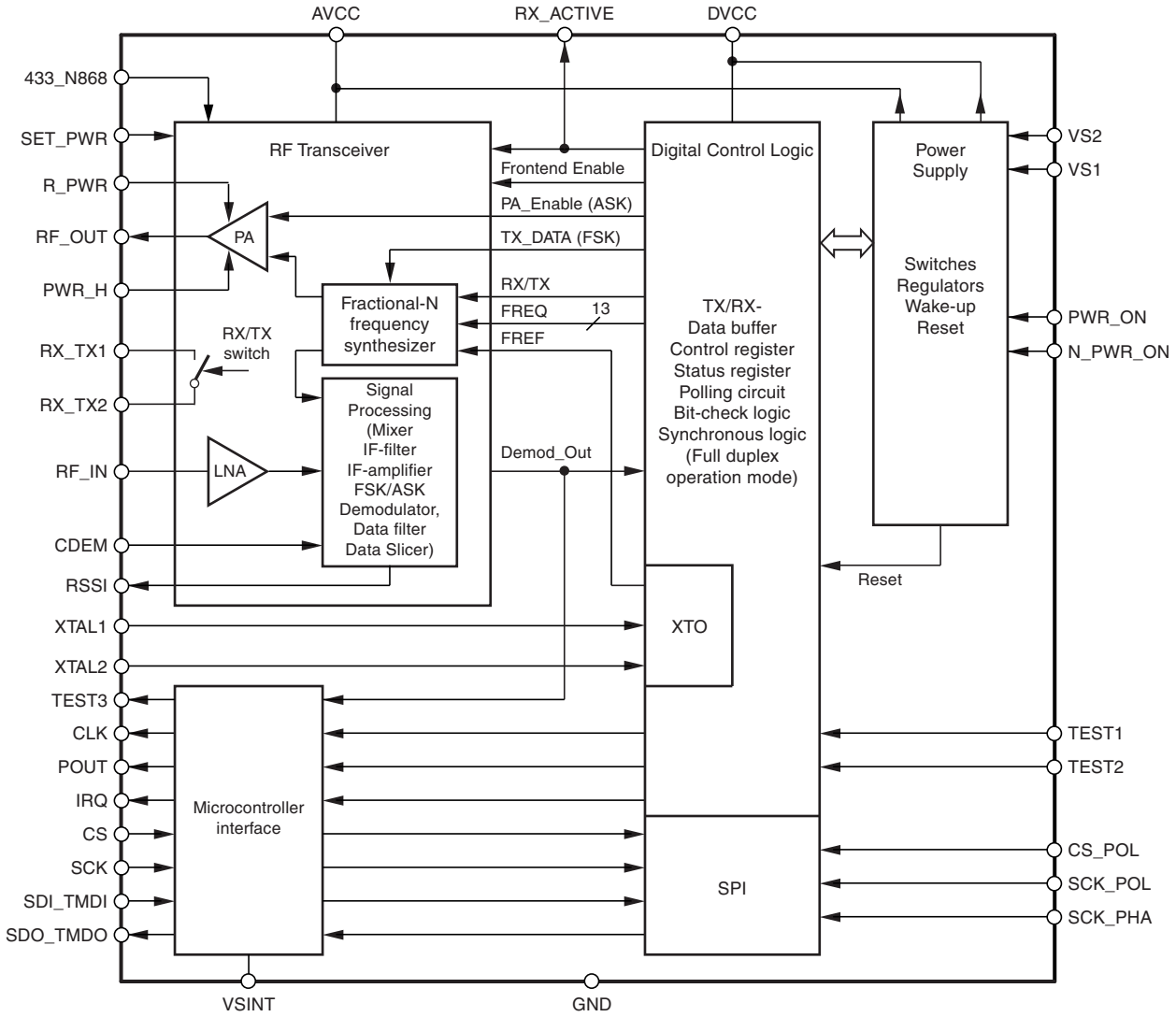
Table 2-1. Pin Description

Pin	Symbol	Function
1	NC	Not connected
2	NC	Not connected
3	NC	Not connected
4	RF_IN	RF input
5	NC	Not connected
6	433_N868	Selects RF input/output frequency range
7	NC	Not connected
8	R_PWR	Resistor to adjust output power
9	PWR_H	Pin to select output power
10	RF_OUT	RF output
11	NC	Not connected
12	NC	Not connected
13	NC	Not connected
14	NC	Not connected
15	NC	Not connected
16	AVCC	Blocking of the analog voltage supply
17	VS2	Power supply input for voltage range 4.4V to 5.6V
18	VS1	Power supply input for voltage range 2.15V to 3.6V
19	SETPWR	Internal Programmable Resistor to adjust output power
20	TEST1	Test input, at GND during operation
21	DVCC	Blocking of the digital voltage supply
22	CS_POL	Select polarity of pin CS
23	TEST2	Test input, at GND during operation
24	XTAL1	Reference crystal
25	XTAL2	Reference crystal
26	NC	Not connected
27	VSINT	Microcontroller interface supply voltage
28	POUT	Programmable output
29	IRQ	Interrupt request
30	CLK	Clock output to connect a microcontroller
31	SDO_TMDO	Serial data out/transparent mode data out
32	SDI_TMDI	Serial data in/transparent mode data in
33	SCK	Serial clock
34	TEST3	Test output open during operation
35	CS	Chip select for serial interface
36	RSSI	Output of the RSSI amplifier
37	CDEM	Capacitor to adjust the lower cut-off frequency data filter
38	RX_TX2	Has to be connected GND
39	RX_TX1	Switch pin to decouple LNA in TX mode (RKE mode)
40	PWR_ON	Input to switch on the system (active high)
41	NC	Not connected

Table 2-1. Pin Description (Continued)

Pin	Symbol	Function
42	NC	Not connected
43	SCK_POL	Polarity of the serial clock
44	SCK_PHA	Phase of the serial clock
45	N_PWR_ON	Keyboard input (can also be used to switch on the system, active low)
46	RX_ACTIVE	Indicates RX operation mode
47	NC	Not connected
48	NC	Not connected
	GND	Ground/Backplane (exposed die pad)

Figure 2-2. Block Diagram



3. Typical Key Fob Application for Bi-directional RKE

Figure 3-1. Typical Key Fob Application for Bi-directional RKE with 5 dBm TX Power, 433.92 MHz

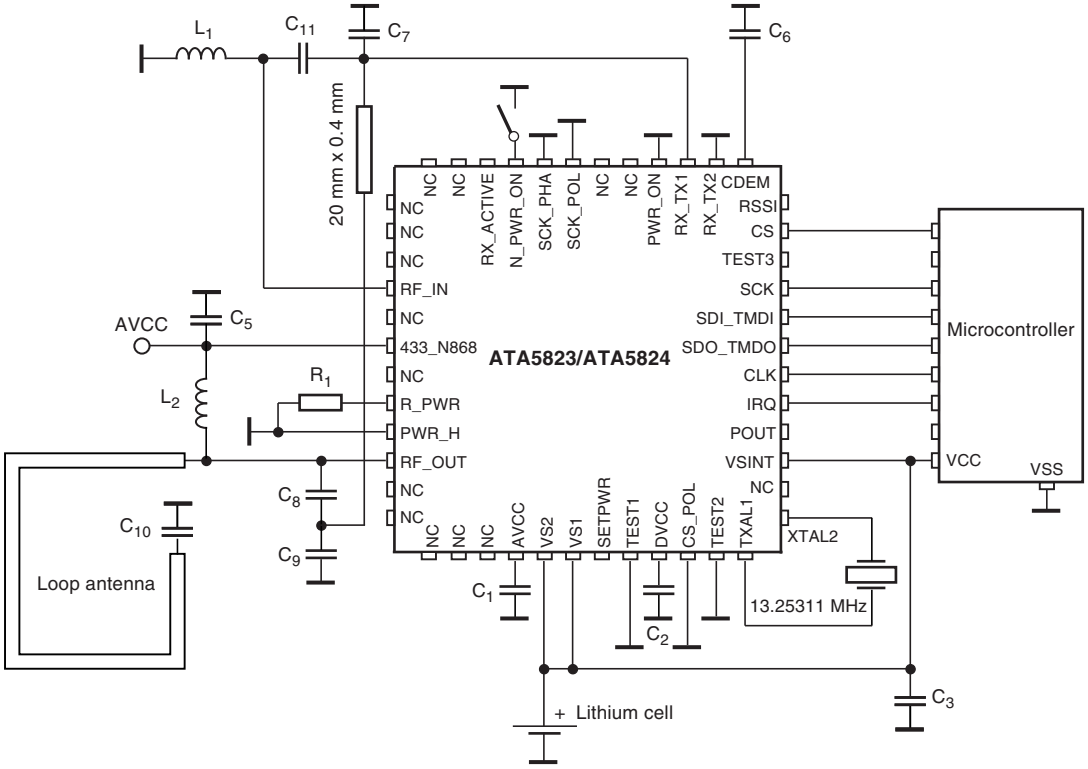


Figure 3-1 shows a typical 433.92 MHz RKE key fob application. The external components are 10 capacitors, 1 resistor, 2 inductors and a crystal. C_1 to C_3 are 68 nF voltage supply blocking capacitors. C_5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1 pF to 33 pF. L_1 is a matching inductor of about 5.6 nH to 56 nH. L_2 is a feed inductor of about 120 nH. A load capacitor of 9 pF for the crystal is integrated. R_1 is typically 22 kΩ and sets the output power to about 5.5 dBm. The loop antenna's quality factor is somewhat reduced by this application due to the quality factor of L_2 and the RX/TX switch. On the other hand, this lower quality factor is necessary to have a robust design with a bandwidth that is wide enough for production tolerances. Due to the single-ended and ground-referenced design, the loop antenna can be a free-form wire around the application as it is usually employed in RKE unidirectional systems. The ATA5823/ATA5824 provides sufficient isolation and robust pulling behavior of internal circuits from the supply voltage as well as an integrated VCO inductor to allow this. Since the efficiency of a loop antenna is proportional to the square of the surrounded area, it is beneficial to have a large loop around the application board with a lower quality factor to relax the tolerance specification of the RF matching components and to get a high antenna efficiency in spite of their lower quality factor.

4. Typical Car Application for Bi-directional RKE

Figure 4-1. Typical Car Application for Bi-directional RKE with 10 dBm TX Power, 433.92 MHz

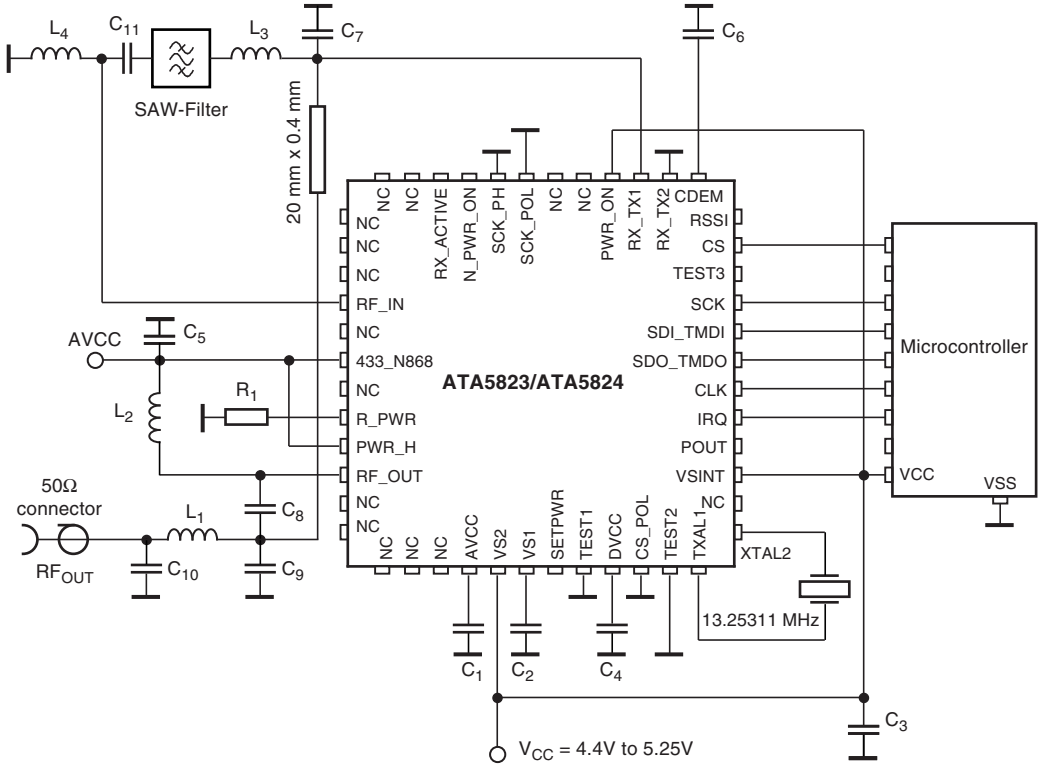


Figure 4-1 shows a typical 433.92 MHz V_{CC} = 4.4V to 5.25V RKE car application. The external components are 11 capacitors, 1 resistor, 4 inductors, a SAW filter and a crystal. C_1, C_3 and C_4 are 68 nF voltage supply blocking capacitors. C_2 is a 2.2 µF supply blocking capacitor for the internal voltage regulator. C_5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{11} are RF matching capacitors in the range of 1 pF to 33 pF. L_2 to L_4 are matching inductors of about 5.6 nH to 56 nH. A load capacitor for the crystal of 9 pF is integrated. R_1 is typically 22 kΩ and sets the output power at RF_{OUT} to about 10 dBm. Since a quarter wave or PCB antenna, which has high efficiency and wideband operation, is typically used here, it is recommended to use a SAW filter to achieve high sensitivity in case of powerful out-of-band blockers. L_1, C_{10} and C_9 together form a low-pass filter, which is needed to filter out the harmonics in the transmitted signal to meet regulations.

5. Typical Key Fob Application for Full-duplex PEG

Figure 5-1. Typical Key Fob Application for Full-duplex PEG, 433.92 MHz

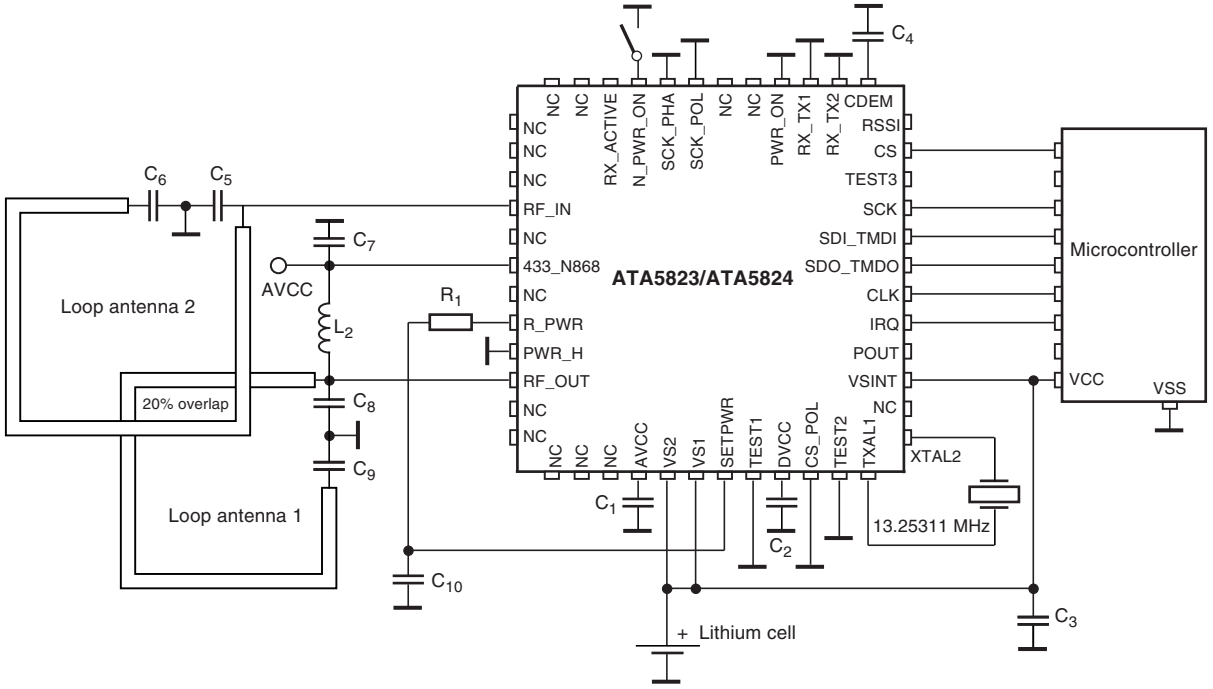


Figure 5-1 shows a typical 433.92 MHz PEG key fob application. The external components are 10 capacitors, 1 resistor, 1 inductor and a crystal. C_1 to C_3 are 68 nF voltage supply blocking capacitors. C_7 is a 10 nF supply blocking capacitor. C_4 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_5, C_6, C_8 and C_9 are RF matching capacitors in the range of 1 pF to 33 pF. L_2 is a feed inductor of about 120 nH. C_{10} is a 10 nF capacitor which is necessary to prevent that signals couple into the pin R_PWR, causing amplitude modulation of the output power and a spurious rise of the transmitted signal. R_1 and C_{10} should be placed close to the R_PWR pin. A load capacitor of 9 pF for the crystal is integrated. R_1 is typically 22 kΩ and SETPWR is programmed to get an output power of –7 dBm in full-duplex mode and 5 dBm in half-duplex mode. The quality factor of the loop antenna 1 is only reduced by the quality factor of L_2, the tolerances of C_9 and C_8 are thus important. The quality factor of the loop antenna 2 is reduced to half due to the loading with the input impedance of RF_IN. With well designed loop antennas and the correct degree of overlapping, the isolation between RF_OUT and RF_IN is about 28 dB and the coupled output power from RF_OUT to RF_IN is about –35 dBm. The decoupling of two loop antennas situated close to each other is due to the effect that the magnetic flux from the part of loop antenna 1 that does not overlap and that of the overlapping part has an opposite direction. Depending on the relative position between the two antennas, a decoupling of 28 dB is achievable. Due to additional capacitive coupling between the loops the position of the components C_5, C_6 and C_8, C_9 are also important. The receive Sensitivity in full-duplex mode is reduced from –106 dBm without coupled RF-Power at RF_IN to –96 dBm with –35 dBm coupled RF power at RF_IN.

6. Typical Car Application for Full-duplex PEG

Figure 6-1. Typical Car Application for Full-duplex PEG, 433.92 MHz

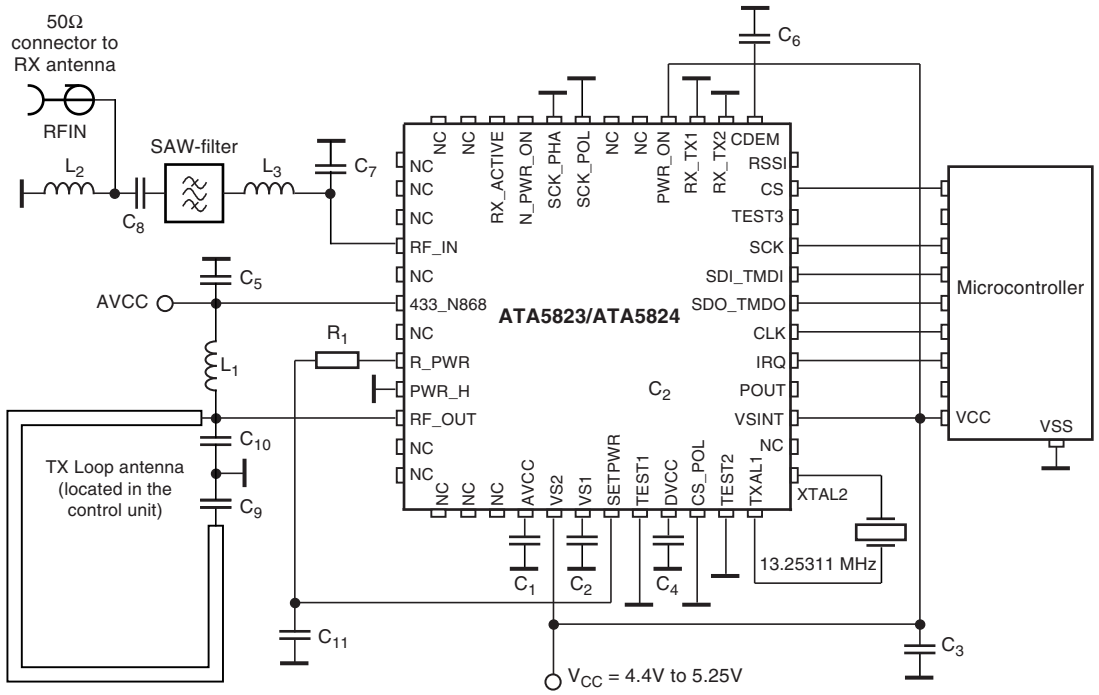


Figure 6-1 shows a typical 433.92 MHz V_{CC} = 4.4V to 5.25V PEG car application. The external components are 11 capacitors, 1 resistor, 3 inductors, a SAW Filter and a crystal. C_1, C_3 and C_4 are 68 nF voltage supply blocking capacitors. C_2 is a 2.2 µF supply blocking capacitors for the internal voltage regulator. C5 is a 10 nF supply blocking capacitor. C_6 is a 15 nF fixed capacitor used for the internal quasi-peak detector and for the high-pass frequency of the data filter. C_7 to C_{10} are RF matching capacitors in the range of 1 pF to 33 pF. L_1 is a feed inductor of about 120 nH, L_2 and L_3 are matching inductors to match the RX-antenna to the SAW and the SAW to RF_IN. A load capacitor of 9 pF for the crystal is integrated. C_{11} is a 10 nF capacitor which is necessary to prevent that signals couple into the pin R_PWR, causing amplitude modulation of the output power and a spurious rise of the transmitted signal. R_1 and C_{11} should be placed close to the R_PWR pin. R_1 is typically 22 kΩ and SETPWR is programmed to get an output power of 0 dBm in full-duplex mode and 5 dBm in half-duplex mode. The quality factor of the TX-loop antenna is only reduced by the quality factor of L_1, the tolerances of C_9 and C_{10} are thus important. Since the 2 Antennas are located at different places the isolation between RF_OUT and RF_IN is about 45 dB and the coupled output power from RF_OUT to RF_IN is about –45 dBm. The receive Sensitivity in full-duplex mode is reduced from –106 dBm without coupled RF power at RF_IN to –102 dBm with –45 dBm coupled RF power at RF_IN. The use of SAW filters in the full-duplex system is unsuitable due to the high group delay which desensitize the receiver.

7. RF Transceiver in Half-duplex Mode

According to Figure 2-2 on page 5, the RF transceiver consists of an LNA (Low-Noise Amplifier), PA (Power Amplifier), RX/TX switch, fractional-N frequency synthesizer and the signal processing part with mixer, IF filter, IF amplifier with analog RSSI, FSK/ASK demodulator, data filter and data slicer.

In receive mode the LNA pre-amplifies the received signal which is converted down to 226 kHz intermediate frequency (IF), filtered and amplified before it is fed into an FSK/ASK demodulator, data filter and data slicer. The RSSI (Received Signal Strength Indicator) signal and the raw digital output signal of the demodulator are available at the pins RSSI and on TEST3 (open drain output). The demodulated data signal Demod_Out is fed into the digital control logic where it is evaluated and buffered as described in section "Digital Control Logic" on page 35.

In transmit mode the fractional-N frequency synthesizer generates the TX frequency which is fed into the PA. In ASK mode the PA is modulated by the signal PA_Enable. In FSK mode the PA is enabled and the signal TX_DATA (FSK) modulates the fractional-N frequency synthesizer. The frequency deviation is digitally controlled and internally fixed to about ±19.5 kHz (see Table 9-1 on page 30 for exact values). The transmit data can also be buffered as described in section "Digital Control Logic" on page 35. A lock detector within the synthesizer ensures that the transmission will only start if the synthesizer is locked.

In half-duplex mode the RX/TX switch can be used to combine the LNA input and the PA output to a single antenna with a minimum of losses. In full-duplex mode more isolation between receive and transmit antenna is needed, therefore two antennas have to be used.

Transparent modes without buffering of RX and TX data are also available to allow protocols and coding schemes other than the internal supported Manchester encoding, like PWM and pulse position coding.

7.1 Low-IF Receiver

The receive path consists of a fully integrated low-IF receiver. It fulfills the sensitivity, blocking, selectivity, supply voltage and supply current specification needed to manufacture an automotive key fob for RKE and PEG systems without the use of a SAW blocking filter (see Figure 3-1 on page 6 and Figure 5-1 on page 8). The receiver can be connected to the roof antenna in the car when using an additional blocking SAW front-end filter as shown in Figure 4-1 on page 7.

At 433.92 MHz the receiver has a typical system noise figure of 6.5 dB, a system I1dBCP of –30 dBm and a system IIP3 of –20 dBm. The signal path is linear for disturbers up to the I1dBCP and there is hence no AGC or switching of the LNA needed to achieve a better blocking performance. This receiver uses an IF of about 226 kHz (see table "Electrical Characteristics" number 2.10 for exact values), the typical image rejection is 30 dB and the typical 3 dB system bandwidth is 220 kHz (f_{IF} = 226 kHz ±110 kHz, f_{lo_IF} = 116 kHz and f_{hi_IF} = 336 kHz). The demodulator needs a signal to noise ratio of 8 dB for 20 Kbit/s Manchester with ±19.5 kHz frequency deviation in FSK mode, thus, the resulting sensitivity at 433.92 MHz is typically –105.5 dBm.

Due to the low phase noise and spurious of the synthesizer in receive mode[1] together with the eighth order integrated IF filter the receiver has a better selectivity and blocking performance than more complex double superhet receivers, without using external components and without numerous spurious receiving frequencies.

Note: 1. –120 dBC/Hz at ±1 MHz and –72 dBC at $\pm f_{XTO}$ at 433.92 MHz

A low-IF architecture is also less sensitive to second-order intermodulation (IIP2) than direct conversion receivers where every pulse or amplitude modulated signal (especially the signals from TDMA systems like GSM) demodulates to the receiving signal band at second-order non-linearities.

7.2 Input Matching at RF_IN

The measured input impedances as well as the values of a parallel equivalent circuit of these impedances can be seen in Table 7-1. The highest sensitivity is achieved with power matching of these impedances to the source impedance of 50Ω.

Table 7-1. Measured Input Impedances of the RF_IN Pin

f_{RF}/MHz	Z_{In}(RF_IN)	R_{In_p}//C_{In_p}
315	(44-j233)Ω	1278Ω//2.1 pF
433.92	(32-j169)Ω	925Ω//2.1 pF
868.3	(21-j78)Ω	311Ω//2.2 pF

The matching of the LNA Input to 50Ω was done with the circuit according to Figure 7-1 and with the values of the matching elements given in Table 7-2. The reflection coefficients were always ≤ –10 dB. Note that value changes of C_1 and L_1 may be necessary to compensate individual board layout parasitics. The measured typical FSK and ASK Manchester code sensitivities with a Bit Error Rate (BER) of 10^{-3} are shown in Table 7-3 on page 12 and Table 7-4 on page 12. These measurements were done with multilayer inductors having quality factors according to Table 7-2, resulting in estimated matching losses of 0.8 dB at 315 MHz, 0.8 dB at 433.92 MHz and 0.7 dB at 868.3 MHz. These losses can be estimated when calculating the parallel equivalent resistance of the inductor with $R_{loss} = 2 \times \pi \times f \times L \times Q_L$ and the matching loss with $10 \log(1+R_{In_p}/R_{loss})$.

With an ideal inductor, for example, the sensitivity at 433.92 MHz/FSK/20 Kbit/s/ ±19.5 kHz/Manchester can be improved from –105.5 dBm to –106.7 dBm. The sensitivity also depends on the values in the registers of the control logic which examines the incoming data stream. The examination limits must be programmed in control registers 5 and 6. The measurements in Table 7-3 and Table 7-4 on page 12 are based on the values of registers 5 and 6 according to Table 14-3 on page 60.

Figure 7-1. Input Matching to 50Ω

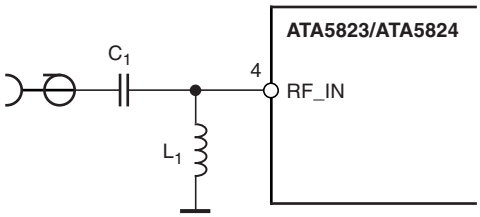


Table 7-2. Input Matching to 50Ω

f_{RF}/MHz	C_1/pF	L_1/nH	Q_{L1}
315	2.4	47	65
433.92	1.8	27	67
868.3	1.2	6.8	50

Table 7-3. Measured Typical Sensitivity 433.92 MHz, FSK, ±19.5 kHz, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0 Kbit/s	BR_Range_0 2.4 Kbit/s	BR_Range_1 5.0 Kbit/s	BR_Range_2 10 Kbit/s	BR_Range_3 20 Kbit/s
315 MHz	–109.5 dBm	–110.0 dBm	–109.0 dBm	–107.5 dBm	–106.5 dBm
433.92 MHz	–108.5 dBm	–109.0 dBm	–108.0 dBm	–106.5 dBm	–105.5 dBm
868.3 MHz	–105.5 dBm	–106.5 dBm	–105.5 dBm	–103.5 dBm	–103.0 dBm

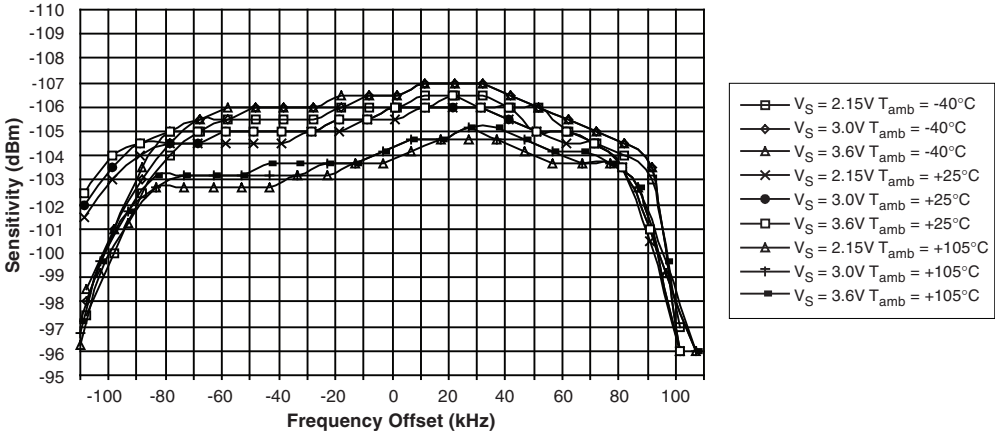
Table 7-4. Measured Typical Sensitivity 433.92 MHz, 100% ASK, Manchester, BER = 10^{-3}

RF Frequency	BR_Range_0 1.0 Kbit/s	BR_Range_0 2.4 Kbit/s	BR_Range_1 5.0 Kbit/s	BR_Range_2 10 Kbit/s
315 MHz	–117.0 dBm	–117.0 dBm	–114.5 dBm	–112.5 dBm
433.92 MHz	–116.0 dBm	–116.0 dBm	–113.5 dBm	–111.5 dBm
868.3 MHz	–113.0 dBm	–113.0 dBm	–111.5 dBm	–109.0 dBm

7.3 Sensitivity versus Supply Voltage, Temperature and Frequency Offset

To calculate the behavior of a transmission system it is important to know the reduction of the sensitivity due to several influences. The most important are frequency offset due to crystal oscillator (XTO) and crystal frequency (XTAL) errors, temperature and supply voltage dependency of the noise figure and IF filter bandwidth of the receiver. Figure 7-2 shows the typical sensitivity at 433.92 MHz/FSK/20 Kbit/s/±19.5 kHz/Manchester versus the frequency offset between transmitter and receiver at T_{amb} = –40°C, +25°C and +105°C and supply voltage $V_S = V_{S1} = V_{S2}$ = 2.15V, 3.0V and 3.6V.

Figure 7-2. Measured Sensitivity 433.92 MHz/FSK/20 Kbit/s/±19.5 kHz/Manchester versus Frequency Offset, Temperature and Supply Voltage



As can be seen in Figure 7-2 on page 12 the supply voltage has almost no influence on the sensitivity. The temperature has an influence of about +1.5/–0.7 dB and a frequency offset of ±85 kHz also influences by about ±1 dB. All these influences, combined with the sensitivity of a typical IC (–105.5dBm), are then within a range of –102.5 dBm and –107 dBm overtemperature, supply voltage and frequency offset. The integrated IF filter has an additional production tolerance of ±10 kHz, hence, a frequency offset between the receiver and the transmitter of ±75 kHz can be accepted for XTAL and XTO tolerances.

Note: For the demodulator used in the ATA5823/ATA5824, the tolerable frequency offset does not change with the data frequency, hence, the value of ±75 kHz is valid for 1 Kbit/s to 20 Kbit/s.

This small sensitivity change over supply voltage, frequency offset and temperature is very unusual in such a receiver. It is achieved by an internal, very fast and automatic frequency correction in the FSK demodulator after the IF filter, which leads to a higher system margin. This frequency correction tracks the input frequency very quickly, if however, the input frequency makes a larger step (e.g., if the system changes between different communication partners), the receiver has to be restarted. This can be done by switching back to IDLE mode and then again to RX mode. For that purpose, an automatic mode is also available. This automatic mode switches to IDLE mode and back into RX mode every time a bit error occurs (see section "Digital Control Logic" on page 35).

7.4 Frequency Accuracy of the Crystals in Bi-directional RKE/PEG

The XTO is an amplitude regulated Pierce type oscillator with integrated load capacitors. The initial tolerances (due to the frequency tolerance of the XTAL, the integrated capacitors on XTAL1, XTAL2 and the XTO's initial transconductance gm) can be compensated to a value within ±0.5 ppm by measuring the CLK output frequency and tuning of f_{RF} by programming the control registers 2 and 3 (see Table 12-7 on page 38 and Table 12-10 on page 39). The XTO then has a remaining influence of less than ±2 ppm overtemperature and supply voltage due to the bandgap controlled gm of the XTO. Thus only 2.5 ppm add to the frequency stability of the used crystals overtemperature and aging.

The needed frequency stability of the used crystals **overtemperature and aging** is hence ±75 kHz/433.92 MHz – 2 × ±2.5 ppm = ±167.84 ppm for 433.92 MHz and ±75 kHz/868.3 MHz – 2 × ±2.5 ppm = ±81.4 ppm for 868.3 MHz. Thus, the used crystals in receiver and transmitter each need to be better than ±83.9 ppm for 433.92 MHz and ±40.7 ppm for 868.3 MHz.

7.5 Frequency Accuracy of the Crystals in a Combined RKE/PEG and TPM System

In a tire pressure measurement system working at 433.92 MHz and using a TPM transmitter ATA5757 and a transceiver ATA5824 as a receiver, the higher frequency tolerances and the tolerance of the frequency deviation of this transmitter has to be considered.

In the TPM transmitter the crystal has an frequency error overtemperature –40°C to +125°C, aging and tolerance of ±80 ppm (±34.7 kHz at 433.92 MHz). The tolerances of the XTO, the capacitors used for FSK-Modulation and the stray capacitors, causing an additional frequency error of ±30 ppm (±13 kHz at 433.92 MHz). The frequency deviation of such a transmitter varies between ±16 kHz and ±24 kHz, since a higher frequency deviation is equivalent to an frequency error, this has to be considered as an additional ±24 kHz – ±19.5 kHz = ±4.5kHz frequency tolerance. All tolerances added, these transmitters have a worst case frequency offset of ±52.2 kHz.

For the transceiver in the car a tolerance of ±75 kHz – ±52.2 kHz = ±22.8 kHz (±52.5 ppm) remains. The needed frequency stability of the used crystals **overtemperature and aging** is ±52.5 ppm – ±2.5 ppm = ±50 ppm. The aging of such a crystal is ±10 ppm leaving reasonable ±40 ppm for the temperature dependency of the crystal frequency in the car.

Since the transceiver in the car is able to receive these TPM transmitter signals with high frequency offsets, the component specification in the key can be largely relaxed.

This system calculation is based on worst case tolerances of all the components, this leads in practice to a system with margin.

For a 315 MHz TPM system using a TPM transmitter ATA5756 and a transceiver ATA5823 as receiver the same calculation must be done, but since the RF frequency is lower, every ppm of crystal tolerances results in less frequency offset and either the system can have higher tolerances or a higher margin there.

For 868 MHz it is not possible to use the transceiver ATA5824 in a combined RKE/PEG and TPM system since all the tolerances double because of the higher RF frequency.

7.6 RX Supply Current versus Temperature and Supply Voltage

Table 7-5 shows the typical supply current at 433.92 MHz of the transceiver in RX mode versus supply voltage and temperature with $V_S = V_{S1} = V_{S2}$. As can be seen the supply current at V_S = 2.15V and T_{amb} = –40°C is less than at V_S = 3V/T_{amb} = 25° which helps to enlarge the battery lifetime within a key fob application because this is also the operation point where a lithium cell has the worst performance. The typical supply current at 315 MHz or 868.3 MHz in RX mode is about the same as for 433.92 MHz.

Table 7-5. Measured 433.92 MHz Receive Supply Current in FSK mode

$V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	8.2 mA	8.8 mA	9.2 mA
T_{amb} = 25°C	9.7 mA	10.3 mA	10.8 mA
T_{amb} = 105°C	11.2 mA	11.9 mA	12.4 mA

7.7 Blocking, Selectivity

As can be seen in Figure 7-3, Figure 7-4 and Figure 7-5 on page 15, the receiver can receive signals 3 dB higher than the sensitivity level in presence of large blockers of –44.5 dBm/-36.0 dBm with small frequency offsets of ±1/ ±10 MHz.

Figure 7-3 and Figure 7-4 on page 15 shows the close-in and narrow-band blocking and Figure 7-5 on page 15 the wide-band blocking characteristic. The measurements were done with a useful signal of 433.92 MHz/FSK/20 Kbit/s/±19.5 kHz/Manchester with a level of –105.5 dBm + 3 dB = –102.5 dBm which is 3 dB above the sensitivity level. The figures show by how much a continuous wave signal can be larger than –102.5 dBm until the BER is higher than 10^{-3}. The measurements were done at the 50Ω input according to Figure 7-1 on page 11. At 1 MHz, for example, the blocker can be 58 dBC higher than –102.5 dBm which is –102.5 dBm +58 dBC = –44.5 dBm. These blocking figures, together with the good intermodulation performance, avoid the additional need of a SAW filter in the key fob application.

Figure 7-3. Close In 3 dB Blocking Characteristic and Image Response at 433.92 MHz

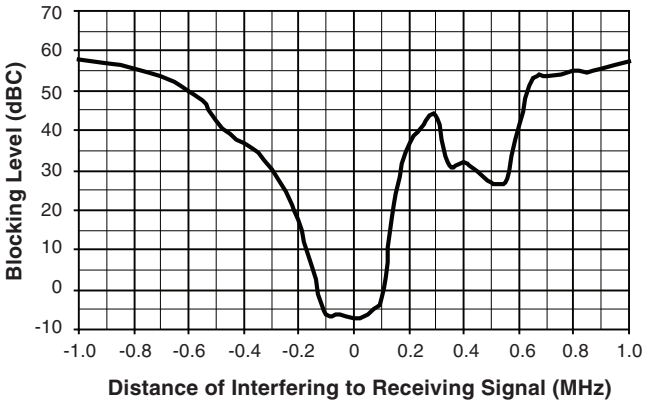


Figure 7-4. Narrow Band 3 dB Blocking Characteristic at 433.92 MHz

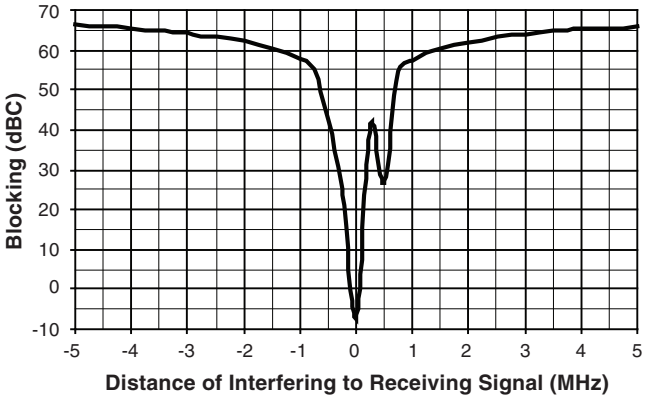


Figure 7-5. Wide Band 3 dB Blocking Characteristic at 433.92 MHz

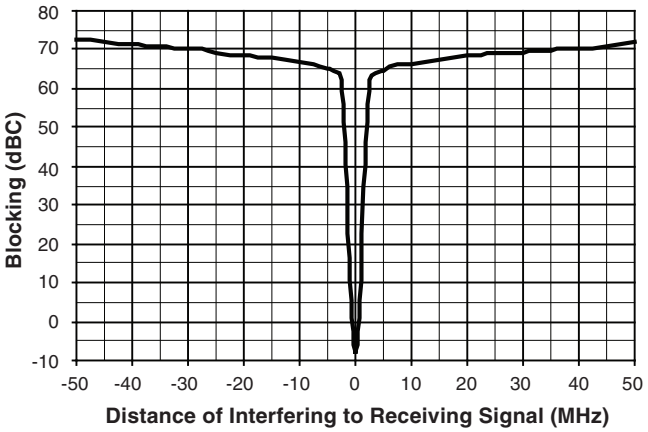


Table 7-6 shows the blocking performance measured relative to –102.5 dBm for some frequencies. Note that sometimes the blocking is measured relative to the sensitivity level –105.5 dBm (denoted dBS) instead of the carrier –102.5 dBm (denoted dBC).

Table 7-6. Blocking 3 dB Above Sensitivity Level with BER < 10^{-3}

Frequency Offset	Blocker Level	Blocking
+0.75 MHz	–47.5 dBm	55.0 dBC/58.0 dBS
–0.75 MHz	–47.5 dBm	55.0 dBC/58.0 dBS
+1.0 MHz	–44.5 dBm	58.0 dBC/61.0 dBS
–1.0 MHz	–44.5 dBm	58.0 dBC/61.0 dBS
+1.5 MHz	–42.0 dBm	60.5 dBC/63.5 dBS
–1.5 MHz	–42.0 dBm	60.5 dBC/63.5 dBS
+10 MHz	–35.5 dBm	67.0 dBC/70.0 dBS
–10 MHz	–35.5 dBm	67.0 dBC/70.0 dBS

The ATA5823/ATA5824 can also receive FSK and ASK modulated signals if they are much higher than the I1dBCP. It can typically receive useful signals at +10 dBm. This is often referred to as the nonlinear dynamic range which is the maximum to minimum receiving signal which is 115.5 dB for 433.92 MHz/FSK/20 Kbit/s/±19.5 kHz/ Manchester. This value is useful if two transceivers have to communicate and are very close to each other.

In a keyless entry system there is another blocking characteristic that has to be considered. A keyless entry system has a typical service range of about 30 m with a receiver sensitivity of about –106 dBm to –109 dBm. In some cases, large blockers limit this service range, and it is important to know how large this blockers can be until the system doesn't work anymore and the user has to use its key. With a recommended sensitivity of about –85 dBm, the system works just around the car. Figure 7-6 and Figure 7-7 on page 17 show the blocking performance in this important case with a useful signal of –85dBm 433.92 MHz/FSK/20 Kbit/s/±19.5 kHz/ Manchester.

As can be seen the system works even with blockers above the compression point. This is due to a wide bandwidth automatic gain control that begins to work if blockers above the compression point are at the antenna input and increasing the current in the LNA/Mixer to get a better compression point needed to handle these large blockers.

Figure 7-6. ±2.5 MHz Blocking Characteristic for –85 dBm Useful Signal at 433.92 MHz

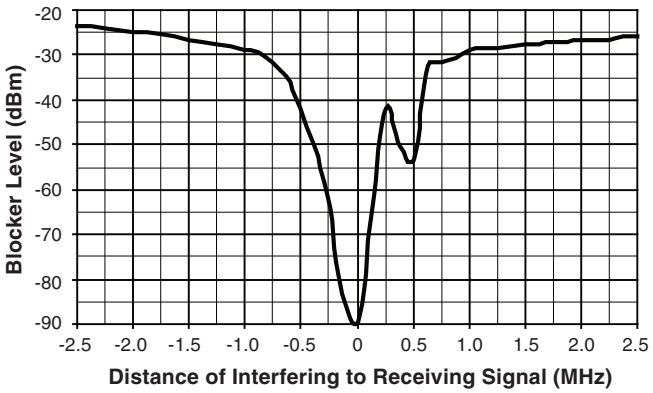
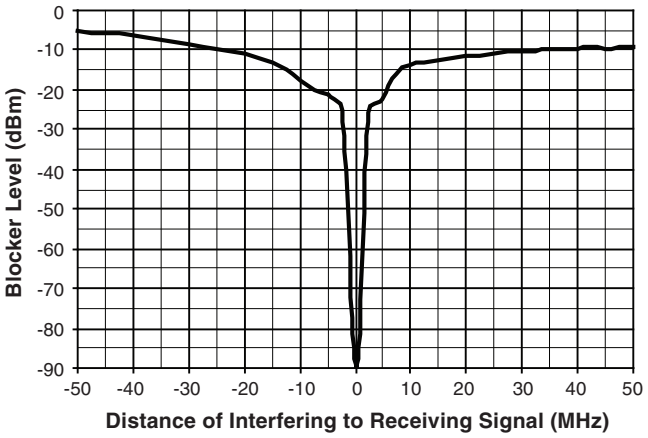


Figure 7-7. ±50 MHz Blocking Characteristic for –85 dBm Useful Signal at 433.92 MHz



This high blocking performance makes it even possible for some applications using quarter wave whip antennas to use a simple LC band-pass filter instead of a SAW filter in the receiver. When designing such a LC filter, take into account that the 3 dB blocking at 433.92 MHz/2 = 216.96 MHz is 42 dBC and at 433.92 MHz/3 = 144.64 MHz is 47 dBC and at 2 × (433.92 MHz + 226 kHz) + –226 kHz = 868.066 MHz/868.518 MHz is 50 dBC. And especially that at 3 × (433.92 MHz + 226 kHz)+226 kHz = 1302.664 MHz the receiver has a second LO harmonic receiving frequency with only 17 dBC blocking.

7.8 Inband Disturbers, Data Filter, Quasi-peak Detector, Data Slicer

If a disturbing signal falls into the received band, or a blocker is not a continuous wave, the performance of a receiver strongly depends on the circuits after the IF filter. Hence the demodulator, data filter and data slicer are important in that case.

The data filter of the ATA5823/ATA5824 implies a quasi-peak detector. This results in a good suppression of above mentioned disturbers and exhibits a good carrier to noise performance. The required ratio of useful signal to disturbing signal, at a BER of 10^{-3} is less than 12 dB in ASK mode and less than 3 dB (BR_Range_0 ... BR_Range_2) and 6 dB (BR_Range_3) in FSK mode. Due to the many different possible waveforms these numbers are measured for signal as well as for disturbers with peak amplitude values. Note that these values are worst case values and are valid for any type of modulation and modulating frequency of the disturbing signal as well as the receiving signal. For many combinations, lower carrier to disturbing signal ratios are needed.

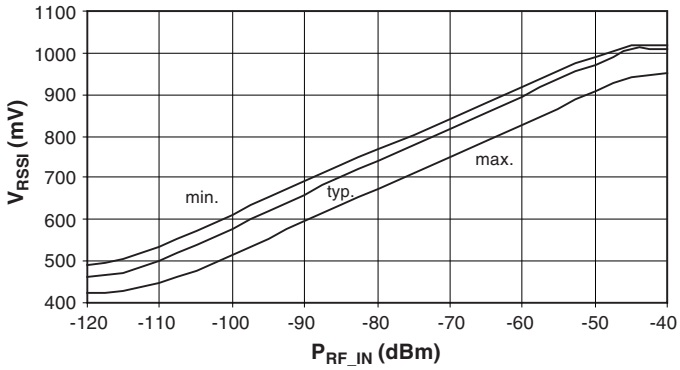
7.9 TEST3 Output

The internal raw output signal of the demodulator Demod_Out is available at pin TEST3. TEST3 is an open drain output and must be connected to a pull-up resistor if it is used (typically 100 kΩ), otherwise no signal is present at that pin. This signal is mainly used for debugging purposes during the setup of a new application, since the received data signal can be seen there without any digital processing.

7.10 RSSI Output

The output voltage of the pin RSSI is an analog voltage, proportional to the input power level. Using the RSSI output signal, the signal strength of different transmitters can be distinguished. The usable dynamic range of the RSSI amplifier is 70 dB, the input power range P_{RFIN} is –115 dBm to –45 dBm and the gain is 8 mV/dB. Figure 7-8 on page 18 shows the RSSI characteristic of a typical device at 433.92 MHz with $V_{S1} = V_{S2}$ = 2.15V to 3.6V and T_{amb} = –40°C to +105°C with a matched input according to Table 7-2 on page 12 and Figure 7-1 on page 11. At 868.3 MHz about 2.7 dB more signal level and at 315 MHz about 1 dB less signal level is needed for the same RSSI results.

Figure 7-8. Typical RSSI Characteristic at 433.92 MHz versus Temperature and Supply Voltage



7.11 Frequency Synthesizer and Channel Selection

The synthesizer is a fully integrated fractional-N design with internal loop filters for receive and transmit mode. The XTO frequency f_{XTO} is the reference frequency FREF for the synthesizer. The bits FR0 to FR12 in control registers 2 and 3 (see Table 12-7 on page 38 and Table 12-10 on page 39) are used to adjust the deviation of f_{XTO}. In half-duplex transmit mode, at 433.92 MHz, the carrier has a phase noise of –111 dBC/Hz at 1 MHz and spurious at FREF of –70 dBC with a high PLL loop bandwidth allowing the direct modulation of the carrier with 20 Kbit/s Manchester data. Due to the closed loop modulation, any spurious caused by this modulation are effectively filtered out as can be seen in Figure 7-11 on page 20. In RX mode the synthesizer has a phase noise of –120 dBC/Hz at 1 MHz and spurious of –72 dBC.

The initial tolerances of the crystal oscillator due to crystal frequency tolerances, internal capacitor tolerances and the parasitics of the board have to be compensated at manufacturing setup with control registers 2 and 3 as can be seen in Table 9-1 on page 30. The other control words for the synthesizer needed for ASK, FSK and receive/transmit switching are calculated internally. The RF (Radio Frequency) resolution is equal to the XTO frequency divided by 16384 which is 777.1 Hz at 315.0 MHz, 808.9 Hz at 433.92 MHz and 818.59 Hz at 868.3 MHz.

The frequency control word FREQ in control registers 2 and 3 can be programmed in the range of 1000 to 6900, hence every frequency within the 433 MHz and 868 MHz ISM bands can be programmed as receive and as transmit frequency and the position of channels within these ISM bands can be chosen arbitrarily (see Table 9-1 on page 30).

Care must be taken regarding the harmonics of the CLK output signal as well as to the harmonics produced by a microprocessor clocked with it, since these harmonics can disturb the reception of signals. In a single channel system using FREQ = 3803 to 4053 ensures that harmonics of this signal, do not disturb the receive mode.

7.12 FSK/ASK Transmission

Due to the fast modulation capability of the synthesizer and the high resolution, the carrier can be internally FSK modulated which simplifies the application of the transceiver. The deviation of the transmitted signal is ±24 digital frequency steps of the synthesizer which is equal to ±18.65 kHz for 315 MHz, ±19.41 kHz for 433.92 MHz and ±19.64 kHz for 868.3 MHz.

Due to closed loop modulation with PLL filtering, the modulated spectrum is very clean, meeting ETSI and CEPT regulations when using a simple LC filter for the power amplifier harmonics as it is shown in Figure 4-1. In ASK mode the frequency is internally connected to the center of the FSK transmission and the power amplifier is switched on and off to perform the modulation. Figure 7-9 to Figure 7-11 on page 20 show the spectrum of the FSK modulation with pseudo-random data with 20 Kbit/s/±19.41 kHz/Manchester and 5 dBm output power.

Figure 7-9. FSK-modulated TX Spectrum (433.92 MHz/20 Kbit/s/±19.41 kHz/Manchester Code)

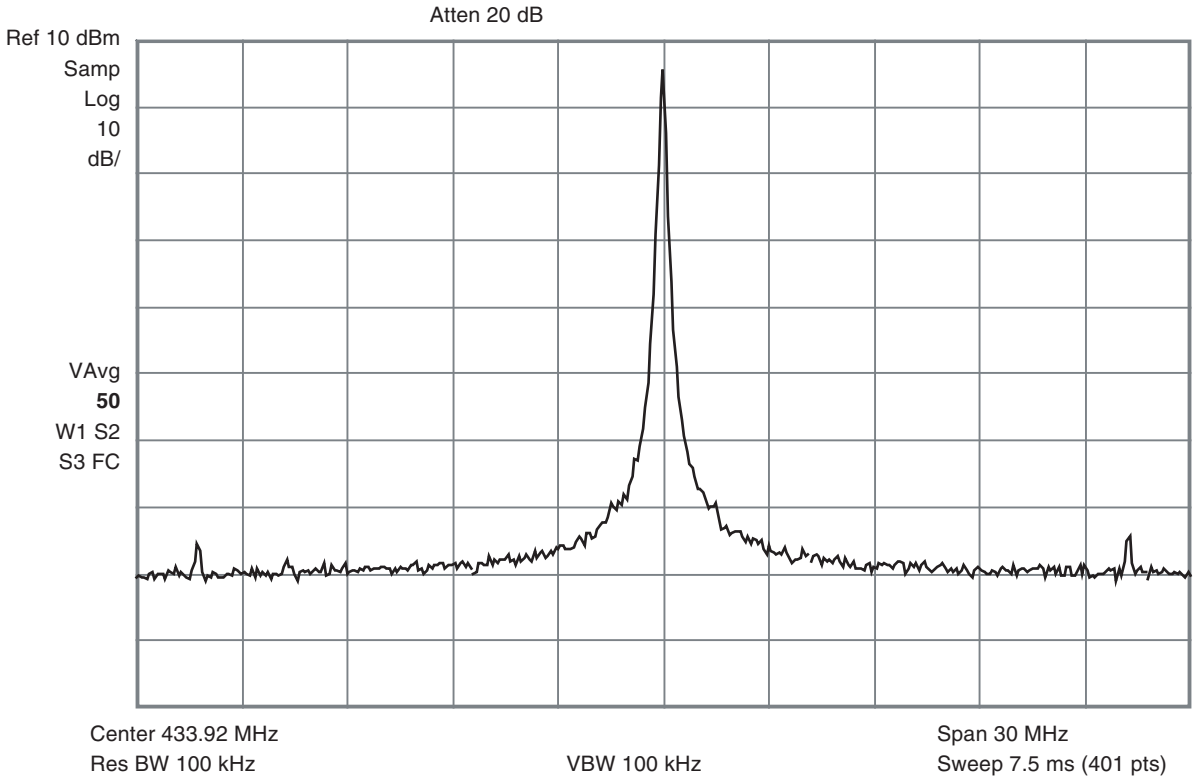


Figure 7-10. Unmodulated TX Spectrum 433.92 MHz - 19.41 kHz (f_{FSK_L})

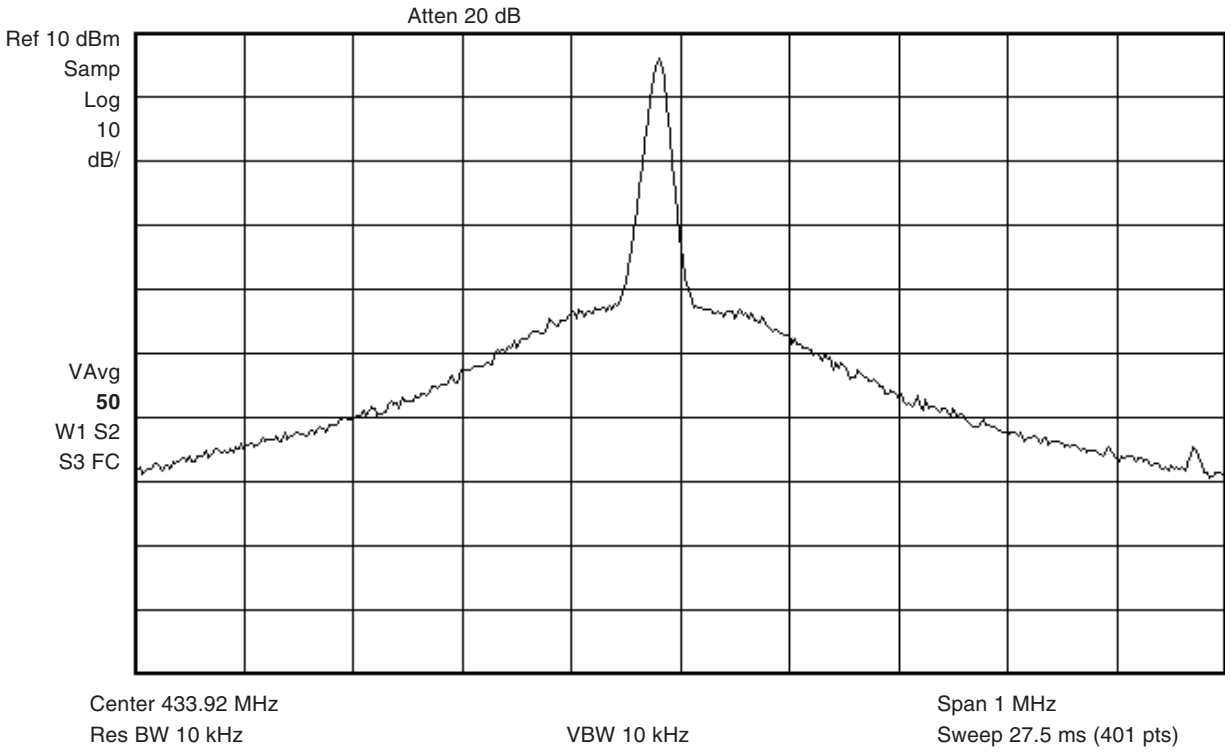
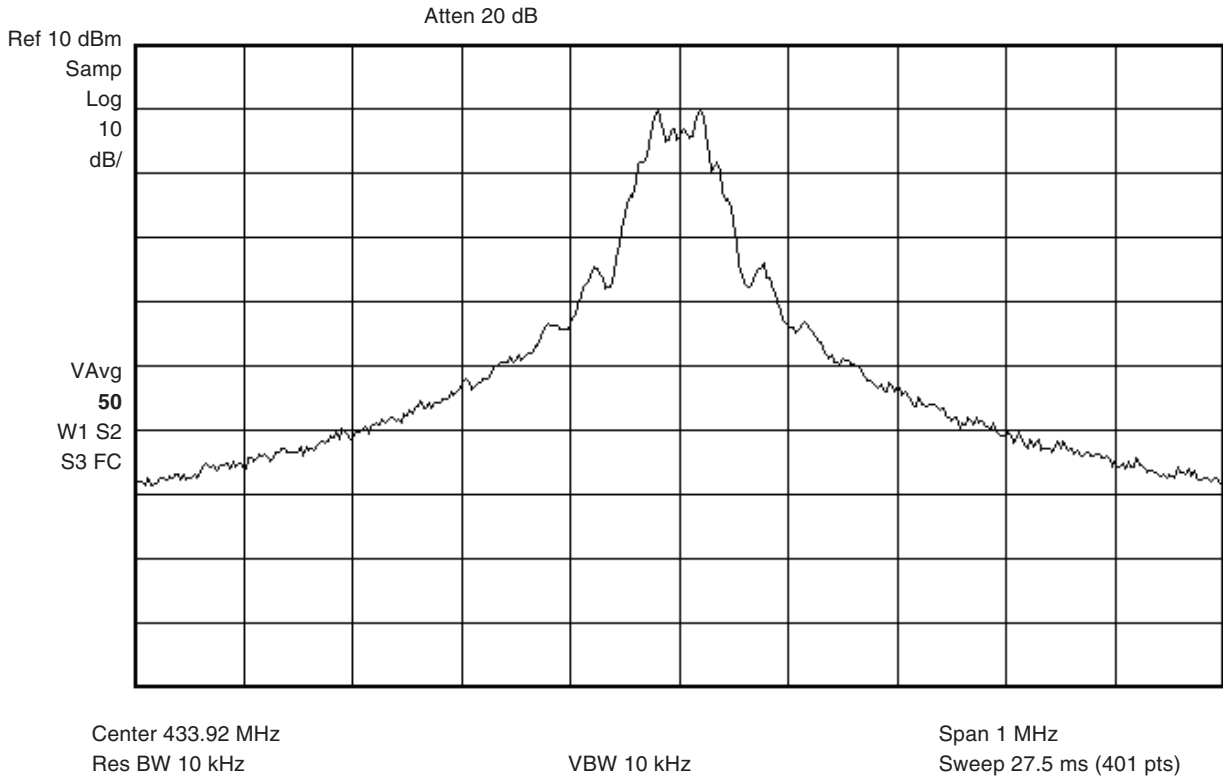


Figure 7-11. FSK-modulated TX Spectrum (433.92 MHz/20 Kbit/s/±19.41 kHz/Manchester Code)



7.13 Output Power Setting and PA Matching at RF_OUT

The Power Amplifier (PA) is a single-ended open collector stage which delivers a current pulse which is nearly independent of supply voltage, temperature and tolerances due to band-gap stabilization. Resistor R_1 (see Figure 7-12 on page 22) sets a reference current which controls the current in the PA. A higher resistor value results in a lower reference current, a lower output power and a lower current consumption of the PA. The usable range of R_1 is 15 kΩ to 56 kΩ. The PWR_H pin switches the output power range between about 0 dBm to 5 dBm (PWR_H = GND) and 5 dBm to 10 dBm (PWR_H = AVCC) by multiplying this reference current with a factor 1 (PWR_H = GND) and 2.5 (PWR_H = AVCC) which corresponds to about 5 dB more output power.

If the PA is switched off in TX mode, the current consumption without output stage and with $V_{S1} = V_{S2} = 3V$, $T_{amb} = 25°C$ is typically 6.5 mA for 868.3 MHz and 6.95 mA for 315 MHz and 433.92 MHz.

The maximum output power is achieved with optimum load resistances R_{Lopt} according to Table 7-7 on page 22. The compensation of the 1.0 pF output capacitance of the RF_OUT pin will be achieved by absorbing it into the matching network, consisting of L_1, C_1, C_3 as shown in Figure 7-12 on page 22. There must be also a low resistive DC path to AVCC to deliver the DC current of the power amplifier's last stage. The matching of the PA output was done with the circuit according to Figure 7-12 on page 22 with the values in Table 7-7. Note that value changes of these elements may be necessary to compensate individual board layout parasitics.

Example:
According to Table 7-7 on page 22, with a frequency of 433.92 MHz and output power of 11 dBm, the overall current consumption is typically 17.8 mA. Hence the PA needs 17.8 mA - 6.95 mA = 10.85 mA in this mode which corresponds to an overall power amplifier efficiency of the PA of $(10^{(11dBm/10)} \times 1\ mW)/(3V \times 10.85\ mA) \times 100\% = 38.6\%$ in this case.

Using a higher resistor in this example of R1 = 1.091 × 22 kΩ = 24 kΩ results in 9.1% less current in the PA of 10.85 mA/1.091 = 9.95 mA and 10 × log(1.091) = 0.38 dB less output power if using a new load resistance of 300Ω × 1.091 = 327Ω. The resulting output power is then 11 dBm – 0.38 dB = 10.6 dBm and the overall current consumption is
6.95 mA + 9.95 mA = 16.9 mA.

The values of Table 7-7 on page 22 were measured with standard multi-layer chip inductors with quality factors Q according to Table 7-7 on page 22.

Looking to the 433.92 MHz/11 dBm case with the quality factor of $Q_{L1} = 43$ the loss in this inductor L_1 is estimated with the parallel equivalent resistance of the inductor $R_{loss} = 2 \times \pi \times f \times L1 \times Q_{L1}$ and the matching loss with 10 log $(1 + R_{Lopt}/R_{loss})$ which is equal to 0.32 dB losses in this inductor. Taking this into account the PA efficiency is then 42% instead of 38.6%.

Be aware that the high power mode (PWR_H = AVCC) can only be used with a supply voltage higher than 2.7V, whereas the low power mode (PWR_H = GND) can be used down to 2.15V as can be seen in the section “Electrical Characteristics: General” on page 72.

The supply blocking capacitor C_2 (10 nF) in Figure 7-12 on page 22 has to be placed close to the matching network because of the RF current flowing through it.

An internal programmable resistor SETPWR is programmable with the control register 8, described in Table 12-25 on page 43. It can be used in conjunction with an external resistor to adjust the output power by connection it like in the application Figure 5-1 on page 8 or Figure 6-1 on page 9. To do that the output power should be adjusted with an external resistor about 50% lower than needed for the target output power and reduced with the programmable resistor during production test until the target power is as close as possible to the target. For example, if using 433.92 MHz at 5 dBm, a resistor of 12k instead of 24k is used and values of PWSET between 25 and 29 can be used to achieve an output power within 5 dBm ±0.5 dB over production. In full-duplex mode this internal resistor is used to reduce the output power for full-duplex operation versus the power in half-duplex operation. Note that this resistor is temperature stable but has tolerances of ±20% and introduces, therefore, additional output power tolerances, it is recommended to adjust output power during the production test if using the SETPWR resistor.

Figure 7-12. Power Setting and Output Matching

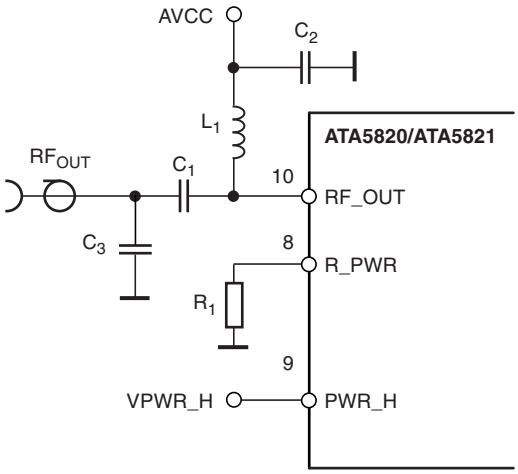


Table 7-7. Measured Output Power and Current Consumption with $V_{S1} = V_{S2} = 3V$, $T_{amb} = 25°C$

Frequency (MHz)	TX Current (mA)	Output Power (dBm)	R1 (kΩ)	VPWR_H	R_{Lopt} (Ω)	L_1 (nH)	Q_{L1}	C_1 (pF)	C_3 (pF)
315	8.5	0.4	56	0	2500	82	28	1.5	0
315	10.5	5.7	27	0	920	68	32	2.2	0
315	16.7	10.5	27	AVCC	350	56	35	3.9	0
433.92	8.6	0.1	56	0	2300	56	40	0.75	0
433.92	11.2	6.2	22	0	890	47	38	1.5	0
433.92	17.8	11	22	AVCC	300	33	43	2.7	0
868.3	9.3	–0.3	33	0	1170	12	58	1.0	3.3
868.3	11.5	5.4	15	0	471	15	54	1.0	0
868.3	16.3	9.5	22	AVCC	245	10	57	1.5	0

7.14 Output Power and TX Supply Current versus Supply Voltage and Temperature

Table 7-8 shows the measurement of the output power for a typical device with $V_{S1} = V_{S2} = V_S$ in the 433.92 MHz and 6.2 dBm case versus temperature and supply voltage measured according to Figure 7-12 on page 22 with components according to Table 7-7 on page 22. As opposed to the receiver sensitivity the supply voltage has here the major impact on output power variations because of the large signal behavior of a power amplifier. Thus a 5V system using the internal voltage regulator shows much less variation than a 2.15V to 3.6V battery system because the AVCC supply voltage is 3.25V ±0.25V for a 5V system.

The reason is that the amplitude at the output RF_OUT with optimum load resistance is AVCC – 0.4V and the power is proportional to $(AVCC – 0.4V)^2$ if the load impedance is not changed. This means that the theoretical output power reduction if reducing the supply voltage from 3.0V to 2.15V is 10 log $((3V – 0.4V)^2/(2.15V – 0.4V)^2)$ = 3.4 dB. Table 7-8 shows that principle behavior in the measurements. This is not the same case for higher voltages, since here, increasing the supply voltage from 3V to 3.6V should theoretical increase the power by 1.8 dB, but only 0.9 dB in the measurements shows that the amplitude does not increase with the supply voltage because the load impedance is optimized for 3V and the output amplitude stays more constant because of the current source nature of the output.

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Table 7-8. Measured Output Power and Supply Current at 433.92 MHz, PWR_H = GND

$V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	9.25 mA 3.2 dBm	10.19 mA 5.5 dBm	10.78 mA 6.2 dBm
T_{amb} = +25°C	10.2 mA 3.4 dBm	11.19 mA 6.2 dBm	11.79 mA 7.1 dBm
T_{amb} = +105°C	10.9 mA 3.0 dBm	12.02 mA 5.4 dBm	12.73 mA 6.3 dBm

Table 7-9 shows the relative changes of the output power of a typical device compared to 3.0V/25°C. As can be seen, a temperature change to –40°C as well as to +105°C reduces the power by less than 1 dB due to the band-gap regulated output current. Measurements of all the cases in Table 7-7 on page 22 overtemperature and supply voltage have shown about the same relative behavior as shown in Table 7-9.

Table 7-9. Measurements of Typical Output Power Relative to 3 V/25°C

$V_S = V_{S1} = V_{S2}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	–3.0 dB	–0.7 dB	0 dB
T_{amb} = +25°C	–2.8 dB	0 dB	+0.9 dB
T_{amb} = +105°C	–3.2 dB	–0.8 dB	+0.1 dB

7.15 RX/TX Switch

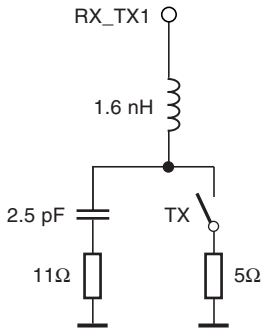
The RX/TX switch decouples the LNA from the PA in TX mode, and directs the received power to the LNA in RX mode. To do this, it has a low impedance to GND in TX mode and a high impedance to GND in RX mode. The pin 38 (RX_TX2) must always be connected to GND in the application. To design a proper RX/TX decoupling a linear simulation tool for radio frequency design together with the measured device impedances of Table 7-1 on page 11, Table 7-7 on page 22, Table 7-10 on page 24 and Table 7-11 on page 25 should be used. The exact element values have to be found on board. Figure 7-13 on page 24 shows an approximate equivalent circuit of the switch. The principal switching operation is described here according to the application of Figure 3-1 on page 6. The application of Figure 4-1 on page 7 works similarly.

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Table 7-10. Impedance of the RX/TX Switch RX_TX2 Shorted to GND

Frequency	Z(RX_TX1) TX mode	Z(RX_TX1) RX mode
315 MHz	(4.8 + j3.2)Ω	(11.3 – j214)Ω
433.92 MHz	(4.5 + j4.3)Ω	(10.3 – j153)Ω
868.3 MHz	(5 + j9)Ω	(8.9 – j73)Ω

Figure 7-13. Equivalent Circuit of the Switch



7.16 Matching Network in TX Mode

In TX mode the 20 mm long and 0.4 mm wide transmission line which is much shorter than λ/4 is approximately switched in parallel to the capacitor C_9 to GND. The antenna connection between C_8 and C_9 has an impedance of about 50Ω looking from the transmission line into the loop antenna with pin RF_OUT, L_2, C_{10}, C_8 and C_9 connected (using a C_9 without the added 7.6 pF capacitor as discussed later). The transmission line can be approximated with a 16 nH inductor in series with a 1.5Ω resistor, the closed switch can be approximated according to Table 7-10 with the series connection of 1.6 nH and 5Ω in this mode. To have a parallel resonant high impedance circuit with little RF power going into it looking, from the loop antenna into the transmission line a capacitor of about 7.6 pF to GND is needed at the beginning of the transmission line (this capacitor is later absorbed into C_9, which is then higher as needed for 50Ω transformation). To keep the 50Ω impedance in RX mode at the end of this transmission line C_7 has to be also about 7.6 pF. This reduces the TX power by about 0.5 dB at 433.92 MHz compared to the case where the LNA path is completely disconnected.

7.17 Matching Network in RX Mode

In RX mode the RF_OUT pin has a high impedance of about 7 kΩ in parallel with 1.0 pF at 433.92 MHz as can be seen in Table 7-11 on page 25. This together with the losses of the inductor L_2 with 120 nH and Q_{L2} = 25 gives about 3.7 kΩ loss impedance at RF_OUT. Since the optimum load impedance in TX mode for the power amplifier at RF_OUT is 890Ω the loss associated with the inductor L_2 and the RF_OUT pin can be estimated to be $10 \times \log(1 + 890/3700) = 0.95$ dB compared to the optimum matched loop antenna without L_2 and RF_OUT. The switch represents, in this mode at 433.92 MHz, about an inductor of 1.6 nH in series with the parallel connection of 2.5 pF and 2.0 kΩ. Since the impedance level at pin RX_TX1 in RX mode is about 50Ω there is only a negligible damping of the received signal by about 0.1 dB. When matching the LNA to the loop antenna the transmission line and the 7.6 pF part of C_9 has to be taken into account when choosing the values of C_{11} and L_1 so that the impedance seen from the loop antenna into the transmission line with the 7.6 pF capacitor connected is 50Ω.

Since the loop antenna in RX mode is loaded by the LNA input impedance the loaded Q of the loop antenna is lowered by about a factor of 2 in RX mode hence the antenna bandwidth is higher than in TX mode.

.

Table 7-11. Impedance RF_OUT Pin in RX mode

Frequency	Z(RF_OUT)RX	R_P//C_P
315 MHz	36Ω –j 502 Ω	7 kΩ/ / 1.0 pF
433.92 MHz	19Ω –j 366 Ω	7 kΩ/ / 1.0 pF
868.3 MHz	2.8Ω –j 141Ω	7 kΩ/ / 1.3 pF

Note that if matching to 50Ω, like in Figure 4-1 on page 7, a high Q wire wound inductor with a Q > 70 should be used for L_2 to minimize its contribution to RX losses which will otherwise be dominant. The RX and TX losses will be in the range of 1.0 dB there.

8. RF Transceiver in Full-duplex Mode

The full-duplex mode of the ATA5823/ATA5824 is intended to be used for the purpose of security against a so called relay attack in passive entry systems. A property of such a passive entry system is that the user has not to push a key fob button like in a keyless entry system. If the user approaches to the door of the car it will wake up the key (in most cases with a low frequency 125 kHz signal) and the communication between the key and the car starts without interaction of the user and afterwards the door opens.

Due to this new feature of the system there is a new possibility of entering a car without permission. One can trigger this communication, take the 125 kHz signal from the car, remodulate it on another carrier and transmit it over a much longer distance than intended by the system. Than receive this signal and remodulate it onto the 125 kHz carrier and retransmit this signal close to the user having the key fob with permission for the car. Such a system is called an RF-Relay and therefore this kind of attack is called relay attack. The high frequency signals of the ATA5823/ATA5824 could be treated the same way if only a half-duplex mode is used within a passive entry system. If using half-duplex RF transceivers, the attacker can switch the direction of the relay with a transmit power detector.

To prevent that the ATA5823/ATA5824 receives and transmit its RF-signals on the same frequency and at the same time. Since the attacker has then to receive and transmit RF signals at the same frequency and time it will be much more difficult to built the hardware for this kind of attack, since its own transmitted output power couples back to its receiver.

This mode works as follows:

Both transceivers transmit FSK with a modulation deviation of half the IF (a frequency deviation of about ±113 kHz), switches the image rejection in the receive path off and uses the transmit frequency as local oscillator for the receiver. If both transceivers send FSK-low or both send FSK-high, the resulting IF is close to zero and is filtered out by the IF-filter. Both receivers receive than a low-signal by using the ASK demodulator as receiver. If the transceivers send different symbols e.g. FSK-low/FSK-high or FSK-high/FSK-low the resulting IF is close to 226 kHz and the ASK demodulator receives a high-signal. Since the transceivers are synchronized at the beginning of the data transfer, they can calculate the transmitted data of the other transceiver from their own transmitted data and the data received from the ASK demodulator.

To use that mode, the received power from the transmitter side of a transceiver should not couple with a to high magnitude to its LNA otherwise the receive path will be desensitized. Therefore, two different antennas for transmit and receive are used with good decoupling (see Figure 5-1 on page 8 and Figure 6-1 on page 9).

Since defined packets are transmitted in FD-mode and the critical point in the transmission is the synchronization and not the data transfer, the sensitivity in FD-mode is defined for packets with 8 bytes of useful data (usually the response from a crypto-challenge response transmission) and for a **P**acket **E**rror **R**ate PER of 5%. For the full-duplex mode the data rate is fixed to 5 Kbit/s

The sensitivity of the receiver in full-duplex mode is dependant on the absolute power value and the phase of the power coupled from the PA to the LNA. Due to the phase dependency, three values are given in the Table 8-1, the first is the typical and the second and third one shows the sensitivity variation.

Table 8-1. Typical Full-duplex Sensitivity Dependent on the Parasitic Received Power and Coupling Phase from the PA 433.92 MHz/Full-duplex Mode/5 Kbit/s PER = 5% at 3V, 25°C

Power from RF_{OUT} at RF_{IN}/dBm	Typical Sensitivity/dBm	Sensitivity Variation/dBm
–30	–91	–88.5/–92.5
–35	–96	–93.5/–97.5
–40	–100	–97.5/–101.5
–45	–103	–100.5/–104.5
–50	–104	–101.5/–105.5

The IC internal decoupling of the RF_{IN} from RF_{OUT} with a power amplifier load impedance optimized for +5dBm is 65 dB on a well designed PCB, hence the coupling is mainly due to the cross-coupling of the antennas.

Table 8-2. Typical Measured Supply Current and Output Power in Full-duplex Mode 433.92 MHz/Power Amplifier is Load Optimized for +5 dBm, R_1 = 22k, PWRSET = 20, (Battery Application)

$V_S = V_{S1} = V_{S2} = V_{SINT}$	2.15V	3.0V	3.6V
T_{amb} = –40°C	10.2 mA/–6.2 dBm	10.9 mA/–5.2 dBm	11.4 mA/–4.6 dBm
T_{amb} = +25°C	11.8 mA/–6.4 dBm	12.5 mA/–5.2 dBm	13.1 mA/–4.5 dBm
T_{amb} = +105°C	13.4 mA/–7.5 dBm	14.2 mA/–5.9 dBm	14.8 mA/–5.0 dBm

Table 8-3. Typical Measured Supply Current and Output Power in Full-duplex Mode/ 433.92 MHz/Power Amplifier is Load Optimized for +5 dBm, R_1 = 22k, PWRSET = 31, (Car Application)

$V_S = V_{S2} = V_{SINT}$	4.4V	5V	5.25V
T_{amb} = –40°C	13.6 mA/3.7 dBm	13.6 mA/3.7 dBm	13.6 mA/3.7 dBm
T_{amb} = +25°C	15.6 mA/4.3 dBm	15.6 mA/4.3 dBm	15.6 mA/4.3 dBm
T_{amb} = +105°C	17.6 mA/ 4.6 dBm	17.6 mA/4.6 dBm	17.6 mA/4.6 dBm

9. XTO

The XTO is an amplitude regulated Pierce oscillator type with integrated load capacitances (2 × 18 pF with a tolerance of ±17%) hence C_{Lmin} = 7.4 pF and C_{Lmax} = 10.6 pF. The XTO oscillation frequency f_{XTO} is the reference frequency FREF for the fractional-N synthesizer. When designing the system in terms of receiving and transmitting frequency offset the accuracy of the crystal and XTO have to be considered.

The synthesizer can adjust the local oscillator frequency for the initial frequency error in f_{XTO}. This is done at nominal supply voltage and temperature with the control registers 2 and 3 (see Table 12-7 on page 38 and Table 12-10 on page 39). The remaining local oscillator tolerance at nominal supply voltage and temperature is then < ±0.5 ppm. The XTO's gm has very low influence of less than ±2 ppm on the frequency at nominal supply voltage and temperature.

In a single channel system less than ±150 ppm should be corrected to avoid that harmonics of the CLK output disturb the receive mode. If the CLK is not used, or carefully layouted on the application PCB (as needed for multi channel systems), more than ±150 ppm can be compensated.

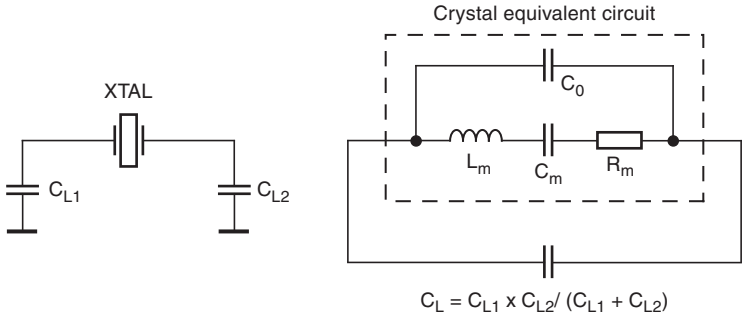
The additional XTO pulling is only ±2 ppm, overtemperature and supply voltage. The XTAL versus temperature and its aging is then the main source of frequency error in the local oscillator.

The XTO frequency depends on XTAL properties and the load capacitances $C_{L1,2}$ at pin XTAL1 and XTAL2. The pulling of f_{XTO} from the nominal f_{XTAL} is calculated using the following formula:

$$P = \frac{C_m}{2} \times \frac{C_{LN} - C_L}{(C_0 + C_{LN}) \times (C_0 + C_L)} \times 10^6 \text{ ppm.}$$

C_m is the crystal's motional, C_0 the shunt and C_{LN} the nominal load capacitance of the XTAL found in its datasheet. C_L is the total actual load capacitance of the crystal in the circuit and consists of C_{L1} and C_{L2} in series connection.

Figure 9-1. XTAL with Load Capacitances



With $C_m \leq 14$ fF, $C_0 \geq 1.5$ pF, $C_{LN} = 9$ pF and $C_L = 7.4$ pF to 10.6 pF the pulling amounts to $P \leq \pm 100$ ppm and with $C_m \leq 7$ fF, $C_0 \geq 1.5$ pF, $C_{LN} = 9$ pF and $C_L = 7.4$ pF to 10.6 pF the pulling is $P \leq \pm 50$ ppm.

Since typical crystals have less than ±50 ppm tolerance at 25°C, the compensation is not critical and can, in both cases, be done with the ±150 ppm.

C_0 of the XTAL has to be lower than $C_{Lmin}/2 = 3.7$ pF for a Pierce oscillator type in order to not enter the steep region of pulling versus load capacitance where there is a risk of an unstable oscillation.

To ensure proper start-up behavior the small signal gain, and thus the negative resistance provided by this XTO at start is very large. For example oscillation starts up, even in worst case, with a crystal series resistance of 1.5 kΩ at $C_0 \leq 2.2$ pF with this XTO. The negative resistance is approximately given by

$$\mathrm{Re}\{Z_{XTOcore}\} = \mathrm{Re}\left\{\frac{Z_1 \times Z_3 + Z_2 \times Z_3 + Z_1 \times Z_2 \times Z_3 \times g_m}{Z_1 + Z_2 + Z_3 + Z_1 \times Z_2 \times g_m}\right\}$$

with Z_1, Z_2 as complex impedances at pin XTAL1 and XTAL2 hence
$Z_1 = -j/(2 \times \pi \times f_{XTO} \times C_{L1}) + 5\Omega$ and $Z_2 = -j/(2 \times \pi \times f_{XTO} \times C_{L2}) + 5\Omega$

Z_3 consists of crystals C_0 in parallel with an internal 110 kΩ resistor hence
$Z_3 = -j/(2 \times \pi \times f_{XTO} \times C_0)$ /110 kΩ, gm is the internal transconductance between XTAL1 and XTAL2 with typically 19 ms at 25°C.

With $f_{XTO} = 13.5$ MHz, gm = 19 ms, $C_L = 9$ pF, $C_0 = 2.2$ pF this results in a negative resistance of about 2 kΩ. The worst case for technological, supply voltage and temperature variations is then for $C_0 \leq 2.2$ pF always higher than 1.5 kΩ.

Due to the large gain at start, the XTO is able to meet a very low start-up time. The oscillation start-up time can be estimated with the time constant τ.

$$\tau = \frac{2}{4 \times \pi^2 \times f_m^2 \times C_m \times (\mathrm{Re}(Z_{XTOcore}) + R_m)}$$

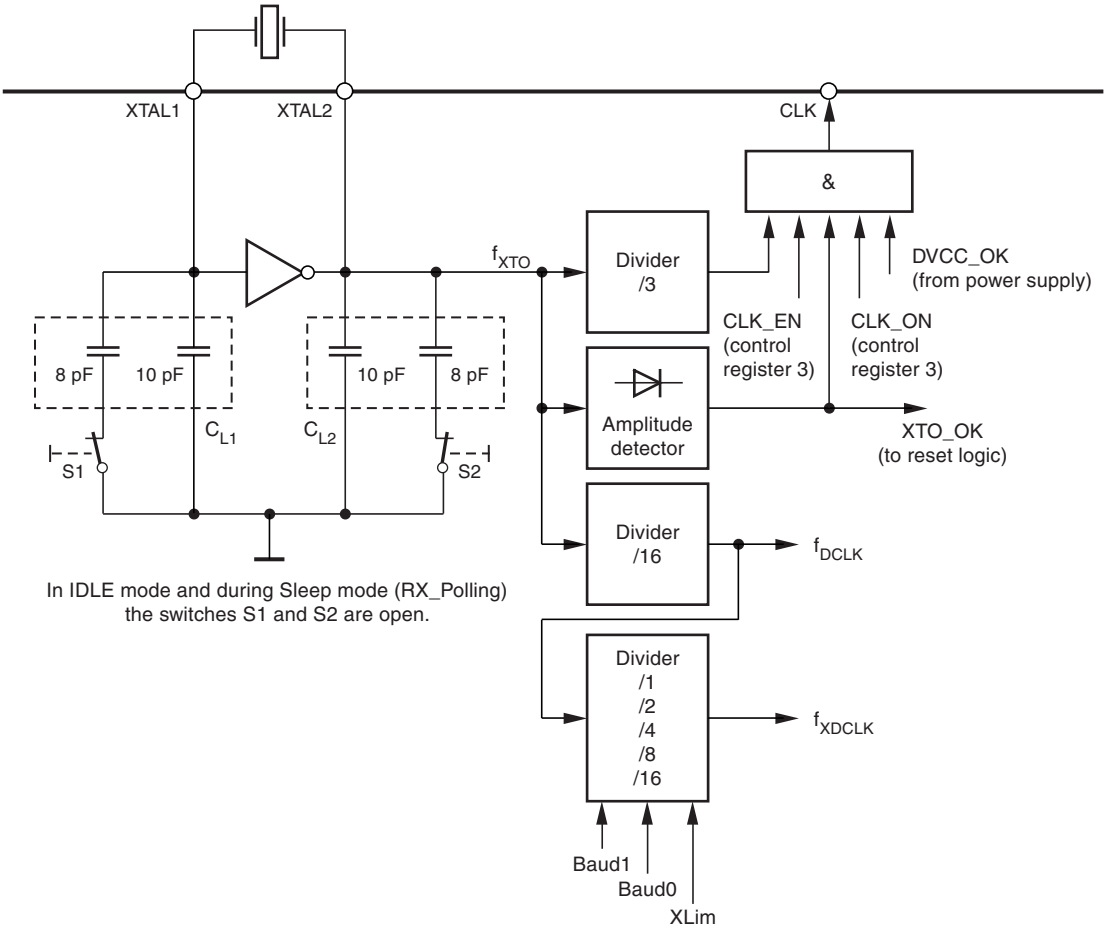
After 10 τ to 20 τ, an amplitude detector detects the oscillation amplitude and sets XTO_OK to High if the amplitude is large enough. This activates the CLK output if CLK_ON and CLK_EN in control register 3 are High (see Table 12-12 on page 39). Note that the necessary conditions of the DVCC voltage also have to be fulfilled (see Figure 9-2 on page 29 and Figure 10-1 on page 31).

To save current in IDLE and Sleep mode, the load capacitors partially are switched off in this modes with S_1 and S_2 seen in Figure 9-2 on page 29.

It is recommended to use a crystal with C_m = 3.0 fF to 7.0 fF, C_{LN} = 9 pF, R_m < 120Ω and C_0 = 1.0 pF to 2.2 pF.

Lower values of C_m can be used, this increases slightly the start-up time. Lower values of C_0 or higher values of C_m (up to 15 fF) can also be used, this has only little influence to pulling.

Figure 9-2. XTO Block Diagram



To find the right values used in the control registers 2 and 3 (see Table 12-7 on page 38 and Table 12-10 on page 39) the relationship between f_{XTO} and the f_{RF} is shown in Table 9-1. To determine the right content, the frequency at pin CLK, as well as the output frequency at RF_OUT in ASK mode can be measured, than the FREQ value can be calculated according to Table 9-1 so that f_{RF} is exactly the desired radio frequency.

Table 9-1. Calculation of f_{RF}

Frequency (MHz)	Pin 6 433_N868	CREG1 Bit(4) FS	f_{XTO} (MHz)	$f_{RF} = f_{TX_ASK} = f_{RX}$	$f_{TX_FSK_L} = f_{TX_FSK_L(FD)}$	$f_{TX_FSK_H}$	$f_{TX_FSK_H(FD)}$	Frequency Resolution
315.0	AVCC	1	12.73193	$f_{XTO} \times \left(24,\ 5 + \frac{FREQ + 24,5}{16384}\right)$	f_{RF} - 18.65 kHz	f_{RF} + 18.65 kHz	f_{RF} + 208.23 kHz	777.1 Hz
868.3	GND	0	13.41180	$f_{XTO} \times \left(64,\ 5 + \frac{FREQ + 24,5}{16384}\right)$	f_{RF} - 19.64 kHz	f_{RF} + 19.64 kHz	f_{RF} + 206.26 kHz	818.6 Hz
433.92	AVCC	0	13.25311	$f_{XTO} \times \left(32,\ 5 + \frac{FREQ + 24,5}{16384}\right)$	f_{RF} - 19.41 kHz	f_{RF} + 19.41 kHz	f_{RF} + 203.74 kHz	808.9 Hz

The variable FREQ depends on the bit PLL_MODE in control register 1 and the parameter FREQ2 and FREQ3, which are defined by the bits FR0 to FR12 in control register 2 and 3 and is calculated as follows:

FREQ = FREQ2 + FREQ3

Care must be taken with the harmonics of the CLK output signal f_{CLK}, as well as to the harmonics produced by an microprocessor clocked with it, since these harmonics can disturb the reception of signals if they get to the RF input. In a single channel system the use of FREQ = 3803 to 4053 ensures that harmonics of this signal do not disturb the receive mode. In a multichannel system the CLK signal can either be not used or carefully layouted on the application PCB. The supply voltage of the microcontroller must also be carefully blocked in a multichannel system.

9.1 Pin CLK

Pin CLK is an output to clock a connected microcontroller. The clock frequency f_{CLK} is calculated as follows:

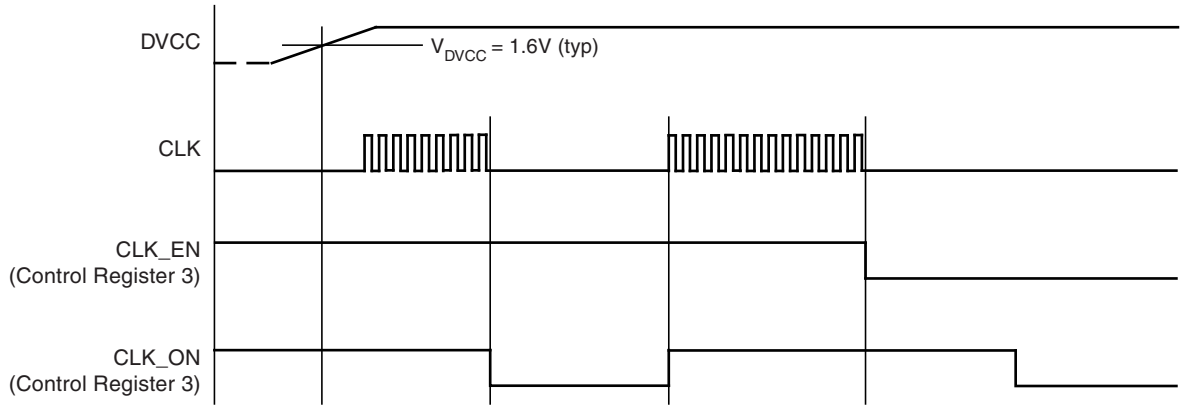
$$f_{CLK} = \frac{f_{XTO}}{3}$$

The signal at CLK output has a nominal 50% duty cycle.

If the bit CLK_EN in control register 3 is set to 0, the clock is disabled permanently.

If the bit CLK_EN is set to 1 and bit CLK_ON (control register 3) is set to 0, the clock is disabled as well. If bit CLK_ON is set to 1 and thus the clock is enabled if the Bit-check is ok (RX, RX Polling, FD mode (Slave)), an event on pin N_PWR_ON occurs or the bit Power_On in the status register is 1.

Figure 9-3. Clock Timing



9.2 Basic Clock Cycle of the Digital Circuitry

The complete timing of the digital circuitry is derived from one clock. According to Figure 9-2 on page 29, this clock cycle T_{DCLK} is derived from the crystal oscillator (XTO) in combination with a divider.

$$f_{DCLK} = \frac{f_{XTO}}{16}$$

T_{DCLK} controls the following application relevant parameters:

- Timing of the polling circuit including bit-check
- TX bit rate

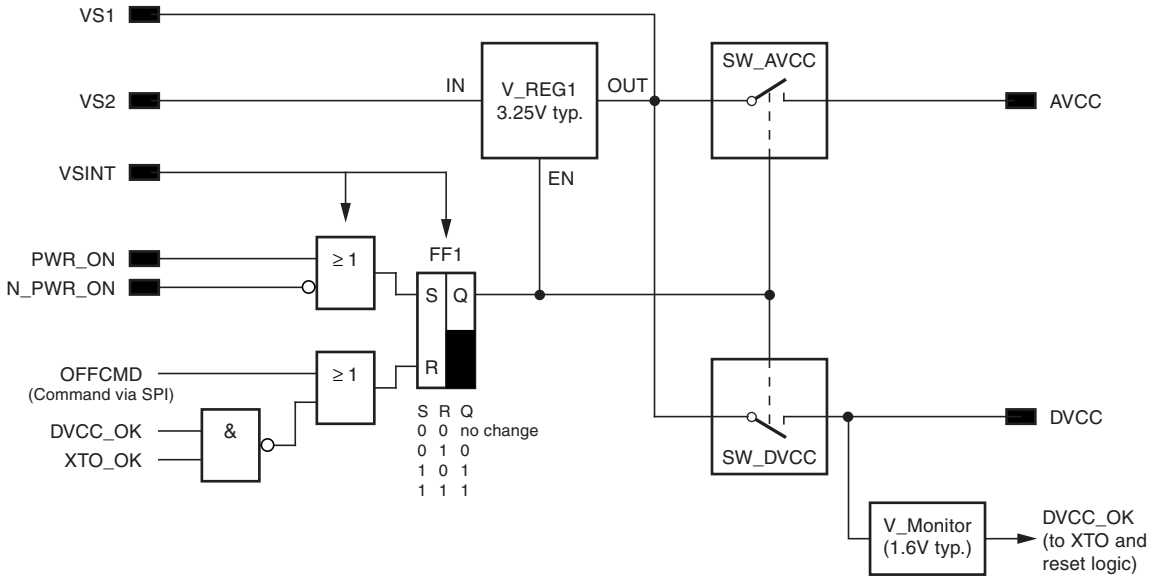
The clock cycle of the Bit-check and the TX bit rate depends on the selected bit-rate range (BR_Range) which is defined in control register 6 (see Table 12-19 on page 41) and X_{Lim} which is defined in control register 4 (see Table 12-16 on page 40). This clock cycle T_{XDCLK} is defined by the following formulas for further reference:

BR_Range ⇒

BR_Range 0: $T_{XDCLK} = 8 \times T_{DCLK} \times X_{Lim}$
BR_Range 1: $T_{XDCLK} = 4 \times T_{DCLK} \times X_{Lim}$
BR_Range 2: $T_{XDCLK} = 2 \times T_{DCLK} \times X_{Lim}$
BR_Range 3: $T_{XDCLK} = 1 \times T_{DCLK} \times X_{Lim}$

10. Power Supply

Figure 10-1. Power Supply



The supply voltage range of the ATA5823/ATA5824 is 2.15V to 3.6V or 4.4V to 5.25V.

Pin VS1 is the supply voltage input for the range 2.15V to 3.6V and is used in battery applications using a single lithium 3V cell. Pin VS2 is the voltage input for the range 4.4V to 5.25V (car applications), in this case the voltage regulator V_REG regulates VS1 to typically 3.25V. If the voltage regulator is active, a blocking capacitor of 2.2 µF has to be connected to VS1.

Pin VSINT is the voltage input for the Microcontroller_Interface and must be connected to the power supply of the microcontroller. The voltage range of V_{VSINT} is 2.25V to 5.25V (see Figure 10-5 and Figure 10-6 on page 35).

AVCC is the internal operation voltage of the RF transceiver and is feed via the switch SW_AVCC by VS1. AVCC must be blocked on pin AVCC with a 68 nF capacitor (see Figure 3-1 on page 6, Figure 4-1 on page 7, Figure 5-1 on page 8 and Figure 6-1 on page 9).

DVCC is the internal operation voltage of the digital control logic and is fed via the switch SW_DVCC by VS1. DVCC must be blocked on pin DVCC with 68 nF (see Figure 3-1 on page 6, Figure 4-1 on page 7, Figure 5-1 on page 8 and Figure 6-1 on page 9).

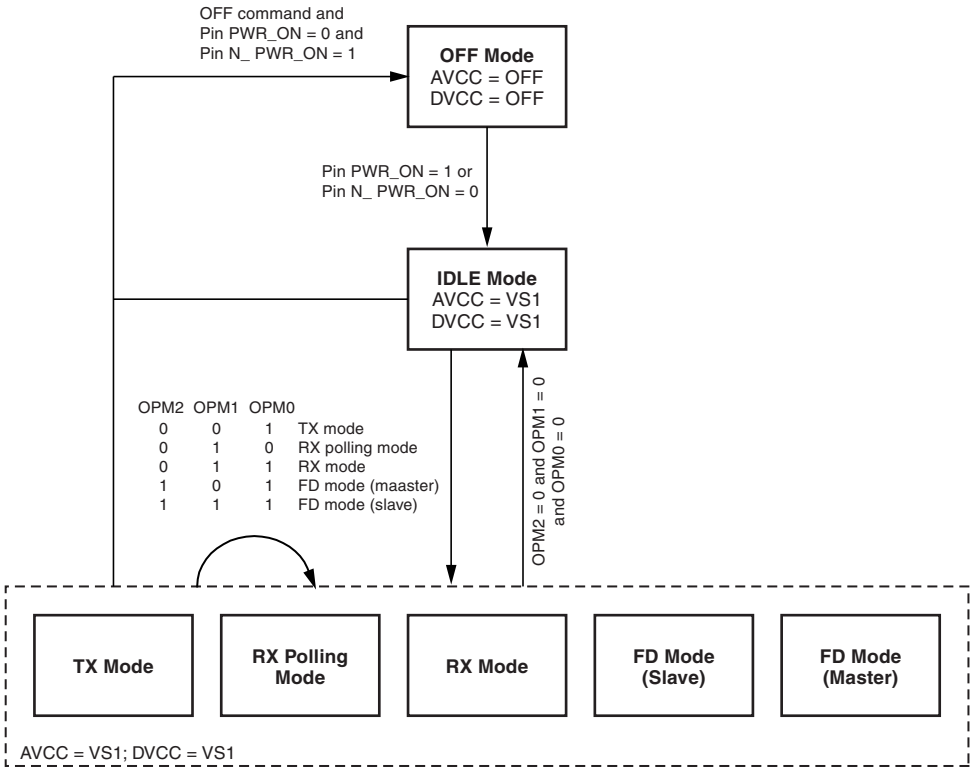
Pin PWR_ON is an input to switch on the transceiver (active high).

Pin N_PWR_ON is an input for a push button and can also be used to switch on the transceiver (active low).

For current consumption reasons it is recommended to set N_PWR_ON to GND only temporarily. Otherwise an additional current flows because of a 50 kΩ pull-up resistor.

A voltage monitor generates the signal DVCC_OK if DVCC ≥ 1.6V typically.

Figure 10-2. Flow Chart Operation Modes



10.1 OFF Mode

After connecting the power supply (battery) to pin VS1 and/or VS2 and VSINT, the transceiver is in OFF mode. In OFF mode AVCC and DVCC are disabled, resulting in very low power consumption (I_{S_OFF} is typically ≤10 nA in the key fob application Figure 3-1 on page 6 and Figure 5-1 on page 8 and ≤0.5 µA in the car application Figure 4-1 on page 7 and Figure 6-1 on page 9). In OFF mode the transceiver is not programmable via the 4-wire serial interface.

10.2 IDLE Mode

In IDLE mode AVCC and DVCC are connected to the battery voltage (VS1).

From OFF mode the transceiver changes to IDLE mode if pin PWR_ON is set to 1 or pin N_PWR_ON is set to 0. This state transition is indicated by an interrupt at pin IRQ and the status bits Power_On = 1 or N_Power_On = 1.

In IDLE mode the RF transceiver is disabled and the power consumption $I_{IDLE_VS1,2}$ is about 270 µA (CLK output OFF VS1 = VS2 = 3V). The exact value of this current is strongly dependent on the application and the exact operation mode, therefore check the section “Electrical Characteristics” for the appropriate application case.

Via the 4-wire serial interface a connected microcontroller can program the required parameter and enable the TX, RX polling, RX or FD mode.The transceiver can be set back to OFF mode by an OFF command via the 4-wire serial interface (the input level of pin PWR_ON must be 0 and pin N_PWR_ON = 1 before writing the OFF command)

Table 10-1. Control Register 1

OPM2	OPM1	OPM0	Function
0	0	0	IDLE mode

10.3 Reset Timing and Reset Logic

If the transceiver is switched on (OFF mode to IDLE mode) DVCC and AVCC are ramping up as illustrated in Figure 10-3. The internal signal DVCC_RESET resets the digital control logic and sets the control register to default values. Bit DVCC_RST in the status register is set to 1.

After V_{DVCC} exceeds 1.6V (typically) and the start-up time of the XTO is elapsed, the output clock at pin CLK is available.

DVCC_RST in the status register is set to 0 if V_{DVCC} exceeds 1.6V, the start-up time of the XTO is elapsed and the status register is read via the 4-wire serial interface.

If V_{DVCC} drops below 1.6V (typically) and pin N_PWR_ON = 1 and pin PWR_ON = 0 the transceiver switches to OFF mode.

Figure 10-3. Reset Timing

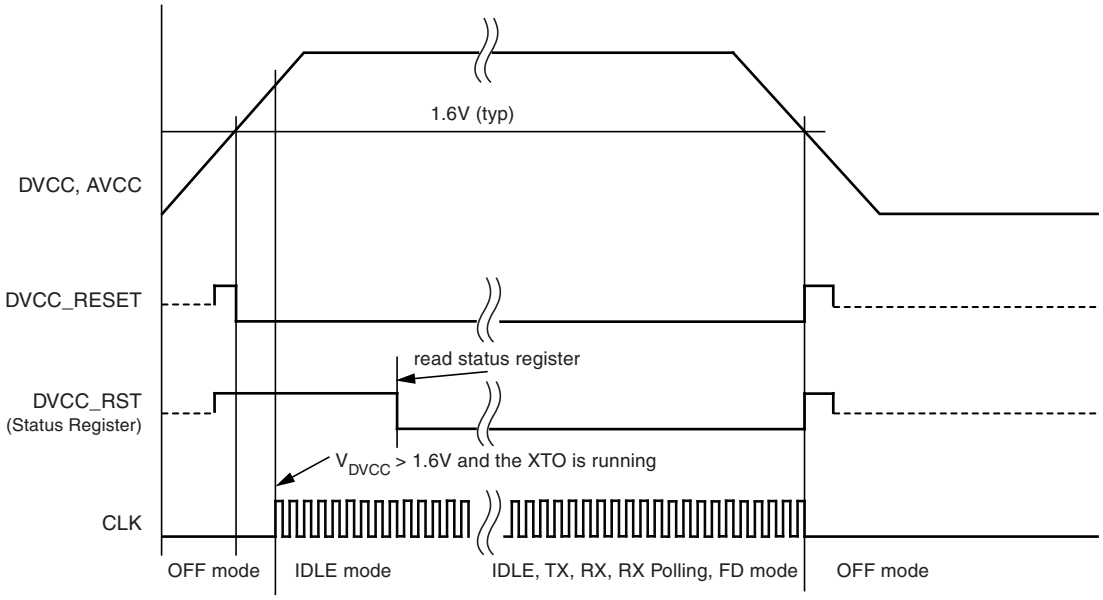
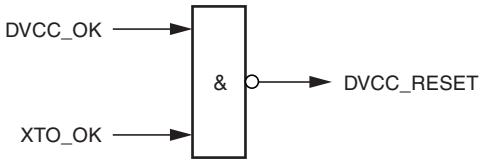


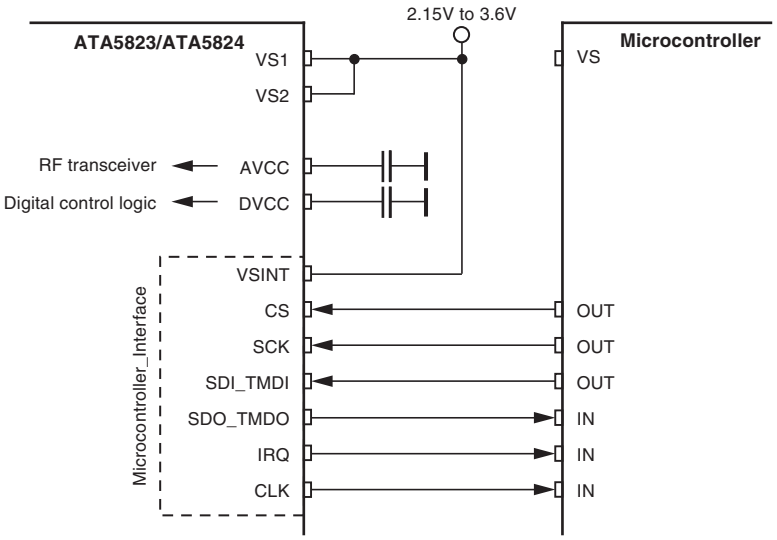
Figure 10-4. Reset Logic



10.4 Battery Application

The supply voltage range is 2.15V to 3.6V.

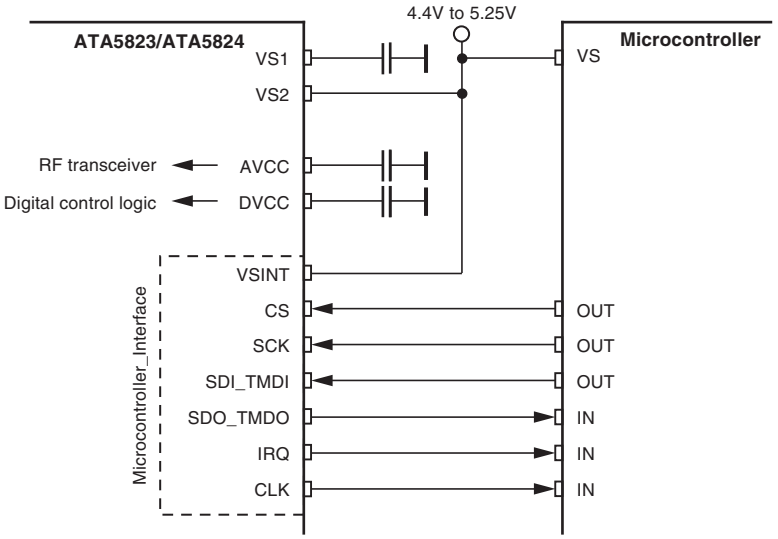
Figure 10-5. Battery Application



10.5 Car Application

The supply voltage range is 4.4V to 5.25V.

Figure 10-6. Car Application



11. Microcontroller Interface

The microcontroller interface is a level converter which converts all internal digital signals which are referred to the DVCC voltage, into the voltage used by the microcontroller. Therefore, the pin VSINT can be connected to the supply voltage of the microcontroller in the case the microcontroller has another supply voltage than the ATA5823/ATA5824.

12. Digital Control Logic

12.1 Register Structure

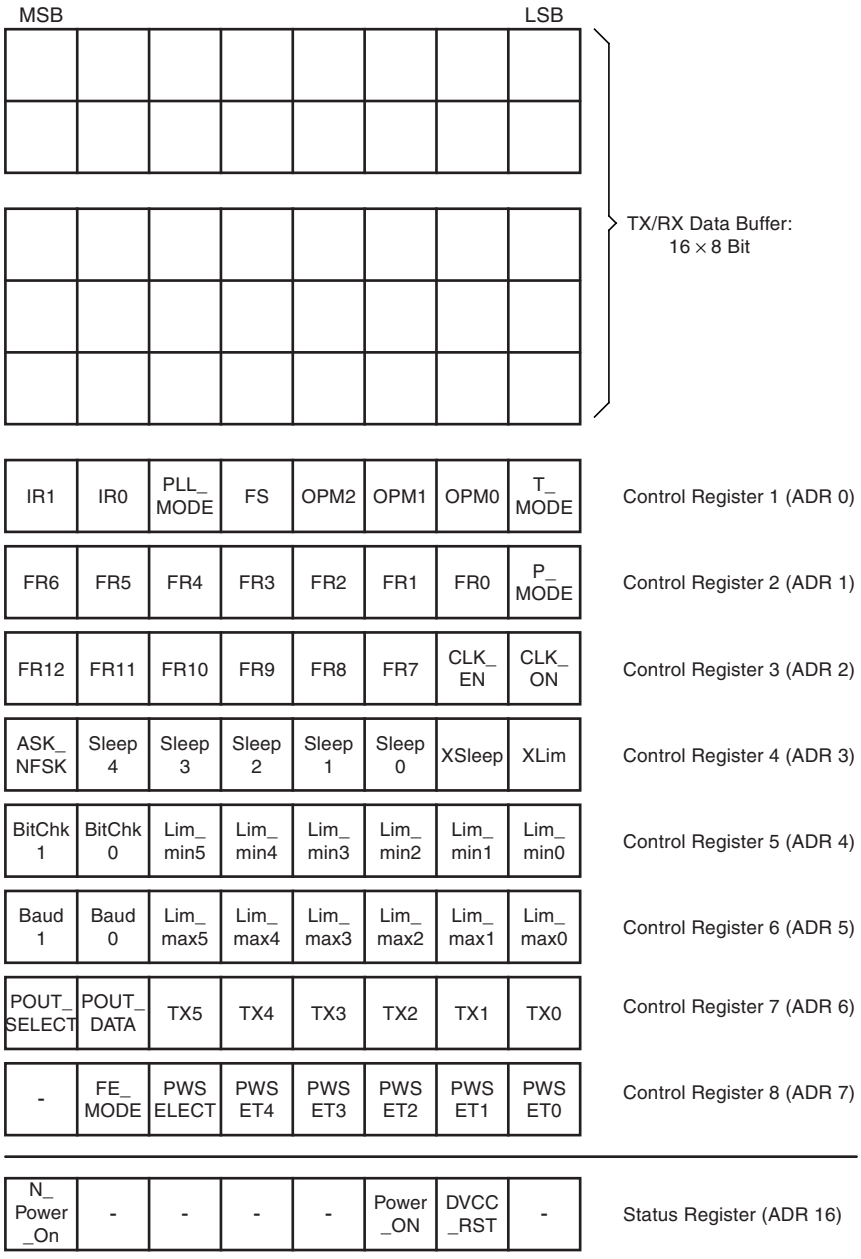
The configuration of the transceiver is stored in RAM cells. The RAM contains a 16 × 8-bit TX/RX data buffer and a 8 × 8-bit Control register and is write and readable via a 4-wire serial interface (CS, SCK, SDI_TMDI, SDO_TMDO).

The 1 × 8-bit status register is not part of the RAM and is readable via the 4-wire serial interface.

The RAM and the status information is stored as long as the transceiver is in any active mode (DVCC = VS1) and gets lost if the transceiver is in the OFF mode (DVCC = OFF).

After the transceiver is turned on via pin PWR_ON = High or pin N_PWR_ON = Low the control registers are in the default state.

Figure 12-1. Register Structure



- = Don't care

12.2 TX/RX Data Buffer

The TX/RX data buffer is used to handle the data transfer during RX and TX operations.

12.3 Control Register

To use the transceiver in different applications the transceiver can be configured by a microcontroller connected via the 4-wire serial interface.

12.3.1 Control Register 1 (ADR 0)

Table 12-1. Control Register 1 (Function of Bit 7 and Bit 6 in RX Mode)

IR1	IR0	Function (RX Mode)
0	0	Pin IRQ is set to 1 if 1 received byte is in the TX/RX data buffer or a receiving error occurred
0	1	Pin IRQ is set to 1 if 2 received bytes are in the TX/RX data buffer or a receiving error occurred
1	0	Pin IRQ is set to 1 if 4 received bytes are in the TX/RX data buffer or a receiving error occurred (default)
1	1	Pin IRQ is set to 1 if 12 received bytes are in the TX/RX data buffer or a receiving error occurred

Table 12-2. Control Register 1 (Function of Bit 7 and Bit 6 in TX Mode)

IR1	IR0	Function (TX Mode)
0	0	Pin IRQ is set to 1 if 1 byte still is in the TX/RX data buffer or the TX data buffer is empty
0	1	Pin IRQ is set to 1 if 2 bytes still are in the TX/RX data buffer or the TX data buffer is empty
1	0	Pin IRQ is set to 1 if 4 bytes still are in the TX/RX data buffer or the TX data buffer is empty (default)
1	1	Pin IRQ is set to 1 if 12 bytes still are in the TX/RX data buffer or the TX data buffer is empty

Note: The Bits IR0 and IR1 have no function in FD mode

Table 12-3. Control Register 1 (Function of Bit 5)

PLL_MODE	Function
0	Adjustable range of FREQ: 3072 to 4095 (default), see Table 12-10 on page 39
1	Adjustable range of FREQ: 0 to 8191, see Table 12-11 on page 39

Table 12-4. Control Register 1 (Function of Bit 4)

FS	Function (RX Mode, TX Mode, FD Mode)
0	Selected frequency 433/868 MHz (default)
1	Selected frequency 315 MHz

Table 12-5. Control Register 1 (Function of Bit 3, Bit 2 and Bit 1)

OPM2	OPM1	OPM0	Function
0	0	0	IDLE mode (default)
0	0	1	TX mode
0	1	0	RX polling mode
0	1	1	RX mode
1	0	0	-
1	0	1	Full-duplex mode (Master)
1	1	0	-
1	1	1	Full-duplex mode (Slave)

Table 12-6. Control Register 1 (Function of Bit 0)

T_MODE	Function
0	TX and RX function via TX/RX data buffer (default)
1	Transparent mode, TX/RX data buffer disabled, TX modulation data stream via pin SDI_TMDI, RX modulation data stream via pin SDO_TMDO

12.3.2 Control Register 2 (ADR 1)

Table 12-7. Control Register 2 (Function of Bit 7, Bit 6, Bit 5, Bit 4, Bit 3, Bit 2 and Bit 1)

FR6 2^6	FR5 2^5	FR4 2^4	FR3 2^3	FR2 2^2	FR1 2^1	FR0 2^0	Function
0	0	0	0	0	0	0	FREQ2 = 0
0	0	0	0	0	0	1	FREQ2 = 1
.	.	.	.	.	.	.	
1	0	1	0	1	0	0	FREQ2 = 84 (default)
.	.	.	.	.	.	.	
1	1	1	1	1	1	1	FREQ2 = 127

Note: Tuning of f_{RF} LSB's (total 13 bits), frequency trimming, resolution of f_{RF} is $f_{XTO}/16384$ which is approximately 800 Hz (see section "XTO", Table 9-1 on page 30)

Table 12-8. Control Register 2 (Function of Bit 0 in RX mode)

P_MODE	Function (RX mode)
0	Pin IRQ is set to 1 if the Bit-check is successful (default)
1	No effect on pin IRQ if the Bit-check is successful

Table 12-9. Control Register 2 (Function of Bit 0 in TX mode)

P_MODE	Function (TX mode)
0	Manchester modulator on (default)
1	Manchester modulator off (NRZ mode)

Note: Bit P_MODE has no function in FD mode

12.3.3 Control Register 3 (ADR 2)

Table 12-10. Control Register 3 (Function of Bit 7, Bit 6, Bit 5, Bit 4, Bit 3 and Bit 2 if Bit PLL_MODE = 0 (in Control Register 1)

FR12 2^{12}	FR11 2^{11}	FR10 2^{10}	FR9 2^{9}	FR8 2^{8}	FR7 2^{7}	Function
X	X	X	0	0	0	FREQ3 = 3072
X	X	X	0	0	1	FREQ3 = 3200
X	X	X	0	1	0	FREQ3 = 3328
X	X	X	0	1	1	FREQ3 = 3456
X	X	X	1	0	0	FREQ3 = 3584
X	X	X	1	0	1	FREQ3 = 3712
X	X	X	1	1	0	FREQ3 = 3840(default)
X	X	X	1	1	1	FREQ3 = 3968

Note: Tuning of f_{RF} MSB's

Table 12-11. Control Register 3 (Function of Bit 7, Bit 6, Bit 5, Bit 4, Bit 3 and Bit 2 if Bit PLL_MODE = 1 (in Control Register 1)

FR12 2^{12}	FR11 2^{11}	FR10 2^{10}	FR9 2^{9}	FR8 2^{8}	FR7 2^{7}	Function
0	0	0	0	0	0	FREQ3 = 0
0	0	0	0	0	1	FREQ3 = 128
0	0	0	0	1	0	FREQ3 = 256
.	.	.	.	.	.	.
0	1	1	1	1	0	FREQ3 = 3840 (default)
.	.	.	.	.	.	.
1	1	1	1	1	0	FREQ3 = 7936
1	1	1	1	1	1	FREQ3 = 8064

Note: Tuning of f_{RF} MSB's

Table 12-12. Control Register 3 (Function of Bit 1 and Bit 0)

CLK_EN	CLK_ON	Function (RX Mode, TX Mode, FD Mode)
0	X	Clock output off (pin CLK)
1	0	Clock output off (pin CLK). Clock switched on by an event: - Bit-check ok or - event on pin N_PWR_ON or - bit Power_On in the status register is 1
1	1	Clock output on (default)

Note: Bit CLK_ON is set to 1 if the Bit-check is ok (RX_Polling, RX mode), an event at pin N_PWR_ON occurs or the bit Power_On in the status register is 1.

12.3.4 Control Register 4 (ADR 3)

Table 12-13. Control Register 4 (Function of Bit 7)

ASK_NFSK	Function (TX Mode, RX Mode)
0	FSK mode (default)
1	ASK mode

Note: Bit ASK_NFSK has no function in FD mode

Table 12-14. Control Register 4 (Function of Bit 6, Bit 5, Bit 4, Bit 3 and Bit 2)

Sleep4 2^4	Sleep3 2^3	Sleep2 2^2	Sleep1 2^1	Sleep0 2^0	Function (RX Mode) Sleep (T_{Sleep} = Sleep × 1024 × T_{DCLK} × X_{Sleep})
0	0	0	0	0	0
0	0	0	0	1	1
.	.	.	.	.	
1	1	0	0	0	24 (T_{Sleep} = 24× 1024 × T_{DCLK} × X_{Sleep}) (default)
.	.	.	.	.	
1	1	1	1	1	31

Note: Bits Sleep0 ... Sleep4 have no function in TX mode and FD mode

Table 12-15. Control Register 4 (Function of Bit 1)

XSleep	Function
0	X_{Sleep} = 1; extended T_{Sleep} off (default)
1	X_{Sleep} = 8; extended T_{Sleep} on

Note: Bit X_{Sleep} has no function in TX mode and FD mode

Table 12-16. Control Register 4 (Function of Bit 0)

XLim	Function
0	X_{Lim} = 1; extended T_{Lim_min}, T_{Lim_max} off (default)
1	X_{Lim} = 2; extended T_{Lim_min}, T_{Lim_max} on

Note: Bit X_{Lim} has no function in TX mode and FD mode

12.3.5 Control Register 5 (ADR 4)

Table 12-17. Control Register 5 (Function of Bit 7 and Bit 6)

BitChk1	BitChk0	Function
0	0	$N_{Bit\text{-}check}$ = 0 (0 bits checked during bit-check)
0	1	$N_{Bit\text{-}check}$ = 3 (3 bits checked during bit-check) (default)
1	0	$N_{Bit\text{-}check}$ = 6 (6 bits checked during bit-check)
1	1	$N_{Bit\text{-}check}$ = 9 (9 bits checked during bit-check)

Note: Bits BitChk0 and BitChk1 have no function in TX mode and FD mode Master

Table 12-18. Control Register 5 (Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0)

Lim_min5 2^5	Lim_min4 2^4	Lim_min3 2^3	Lim_min2 2^2	Lim_min1 2^1	Lim_min0 2^0	Function (RX Mode, FD Mode Slave) Lim_min (Lim_min < 10 are not Applicable) ($T_{Lim_min} = Lim_min \times T_{XDCLK}$)
0	0	1	0	1	0	10
0	0	1	0	1	1	11 ($T_{Lim_min} = 11 \times T_{XDCLK}$) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

Bits Lim_min0 to Lim_min5 have no function in TX mode and FD mode Master.

12.3.6 Control Register 6 (ADR 5)

Table 12-19. Control Register 6 (Function of Bit 7 and Bit 6)

Baud1	Baud0	Function (RX Mode, TX Mode, FD Mode)
0	0	Bit-rate range 0 (B0) 1.0 Kbit/s to 2.5 Kbit/s; $T_{XDCLK} = 8 \times T_{DCLK} \times X_{Lim}$
0	1	Bit-rate range 1 (B1) 2.0 Kbit/s to 5.0 Kbit/s; $T_{XDCLK} = 4 \times T_{DCLK} \times X_{Lim}$ Bit-rate in FD mode = $1 / (168 \times T_{DCLK})$
1	0	Bit-rate range 2 (B2) 4.0 Kbit/s to 10.0 Kbit/s; $T_{XDCLK} = 2 \times T_{DCLK} \times X_{Lim}$ (default)
1	1	Bit-rate range 3 (B3) 8.0 Kbit/s to 20.0 Kbit/s; $T_{XDCLK} = 1 \times T_{DCLK} \times X_{Lim}$ Note that the receiver is not working with >10 Kbit/s in ASK mode

Table 12-20. Control Register 6 (Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0)

Lim_max5 2^5	Lim_max4 2^4	Lim_max3 2^3	Lim_max2 2^2	Lim_max1 2^1	Lim_max0 2^0	Function (RX Mode, FD Mode Slave) Lim_max (Lim_max < 12 are not Applicable) ($T_{Lim_max} = (Lim_max - 1) \times T_{XDCLK}$)
0	0	1	1	0	0	12
0	0	1	1	0	1	13
.	.	.	.	.	.	
1	0	0	0	0	0	32 ($T_{Lim_max} = (32 - 1) \times T_{XDCLK}$) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

Note: Bits Lim_max0 to Lim_max5 have no function in TX mode and FD mode Master

12.3.7 Control Register 7 (ADR 6)

Table 12-21. Control Register 7 (Function of Bit 7 and Bit 6)

POUT_SELECT	POUT_DATA	Function (RX Mode, TX Mode, FD Mode)
0	0	Output level on pin POUT = 0 (default)
0	1	Output level on pin POUT = 1
1	X	Output level on pin POUT = N_RX_ACTIVE(1)

Note: 1. IDLE, TX, FD mode: N_RX_ACTIVE = 1
RX mode: N_RX_ACTIVE = 0

Table 12-22. Control Register 7(Function of Bit 5, Bit 4, Bit 3, Bit 2, Bit 1 and Bit 0)

TX5 2^5	TX4 2^4	TX3 2^3	TX2 2^2	TX1 2^1	TX0 2^0	Function (TX Mode) TX (TX < 10 are not Applicable) (TX_Bitrate = 1/(TX + 1) × T_{XDCLK} × 2)
0	0	1	0	1	0	10
0	0	1	0	1	1	11
.	.	.	.	.	.	
0	1	0	1	0	0	20 (TX_Bitrate = 1/(20 + 1) × T_{XDCLK} × 2) (default)
.	.	.	.	.	.	
1	1	1	1	1	1	63

Note: Bits TX0 to TX5 have no function in RX mode and FD mode

12.3.8 Control Register 8 (ADR 7)

Table 12-23. Control Register 8 (Function of Bit 6)

FE_mode	Function
0	For future use
1	Bit for internal use, must always set to 1 (default)

Table 12-24. Control Register 8 (Function of Bit 5)

PWSELECT	Function (TX Mode, FD Mode)
0	R_{PWSET} = 140Ω typically in TX-mode and as defined by the bits PWSET0 to PWSET4 in FD mode (default)
1	R_{PWSET} as defined by the bits PWSET0 to PWSET4

Table 12-25. Control Register 8 (Function of Bit 4, Bit 3, Bit 2, Bit 1, Bit 0)

PWSET4 2^4	PWSET3 2^3	PWSET2 2^2	PWSET1 2^1	PWSET0 2^0	**Function (TX Mode, FD Mode)** (SETPWR: Programmable internal resistor to reduce the output power in FD and TX mode) **PWSET** SETPWR = 800Ω + (31 – PWSET) × 3 kΩ (typically)
0	0	0	0	0	0
0	0	0	0	1	1
.	.	.	.	.	
1	0	0	0	0	16 (default) SETPWR = 800Ω + (31 – 16) × 3 kΩ (typically)
.	.	.	.	.	
1	1	1	1	0	30
1	1	1	1	1	31

Normally the SETPWR resistor at pin 19 is used in full-duplex mode to decrease the output power until the level at RF_IN is low enough for reception of signals (PWSELECT = 0). With PWSELECT = 1 this resistor can also be used in normal half-duplex TX operation to adjust the output power for production tolerances.

12.3.9 Status Register (ADR 16)

The status register indicates the current status of the transceiver and is readable via the 4-wire serial interface. Setting Power_On or an event on N_Power_On is indicated by an IRQ.

Reading the status register resets the bits Power_On, DVCC_RST and the IRQ.

Table 12-26. Status Register

Status Bit	Function
N_Power_On	Status of pin N_PWR_On Pin N_PWR_ON = 0 → N_Power_On = 1 Pin N_PWR_ON = 1 → N_Power_On = 0 (Figure 12-3 on page 45)
Power_On	Indicates that the transceiver was woken up by pin PWR_ON (rising edge on pin PWR_ON). During Power_On = 1, the bit CLK_ON in control register 3 is set to 1 (Figure 12-4 on page 46).
DVCC_RST	DVCC_RST is set to 1 if the supply voltage of the RAM (V_{DVCC}) was too low and the information in the RAM may be lost. DVCC_RST = 0 → supply voltage of the RAM ok DVCC_RST = 1 → supply voltage of the RAM was too low (typically V_{DVCC} < 1.6V) If the transceiver changes from OFF mode to IDLE mode, DVCC_RST will be set to 1. Reading the Status register resets DVCC_RST to 0.

12.4 Pin N_PWR_ON

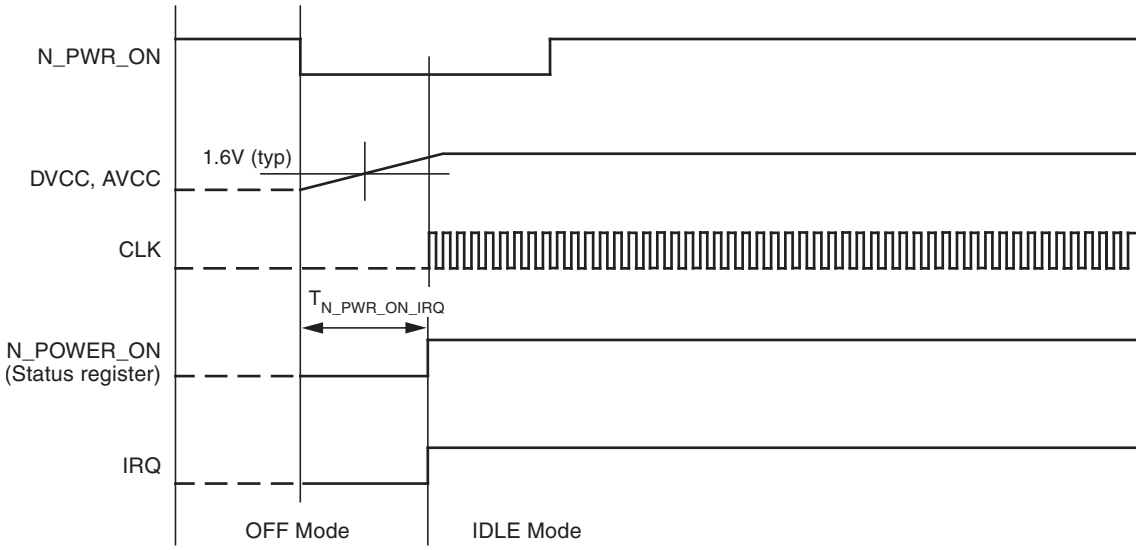
To switch the transceiver from OFF to IDLE mode, pin N_PWR_ON must be set to 0 (maximum $0.2 \times V_{VS2}$) for at least $T_{N_PWR_ON_IRQ}$ (see Figure 12-2). The transceiver recognizes the negative edge and switches on DVCC and AVCC.

If V_{DVCC} exceeds 1.6V (typically) and the XTO is settled, the digital control logic is active and sets the status bit N_Power_On to 1, an interrupt is issued ($T_{N_PWR_ON_IRQ}$) and the output clock on pin CLK is available.

If the level on pin N_PWR_ON was set to 1 before the interrupt is issued, the transceiver stays in OFF mode.

Note: It is not possible to set the transceiver to OFF-mode by setting pin N_PWR_ON to 1. If pin N_PWR_ON is not used, it should be left open because of the internal pull-up resistor

Figure 12-2. Timing Pin N_PWR_ON, Status Bit N_Power_On



If the transceiver is in any of the active modes (IDLE, TX, RX, RX_Polling, FD), an integrated debounce logic is active. If there is an event on pin N_PWR_ON, a debounce counter is set to 0 (T = 0) and started. The status is updated, an interrupt is issued and the debounce counter is stopped after reaching the counter value $T = 8195 \times T_{DCLK}$.

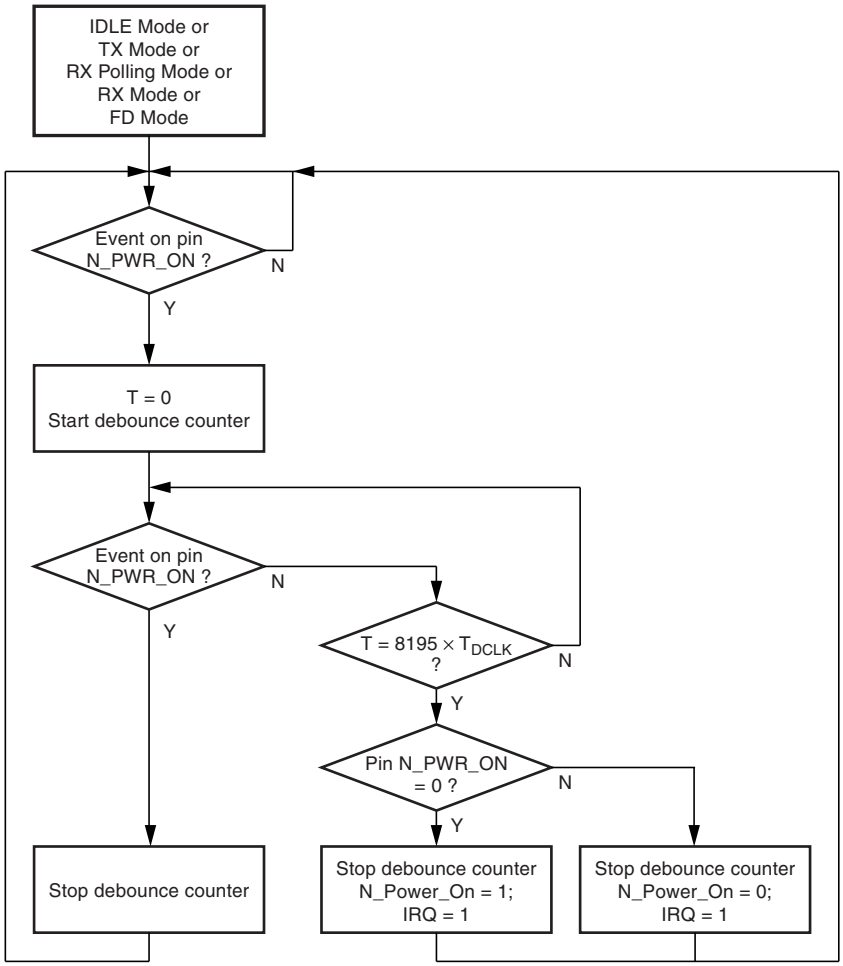
An event on N_PWR_ON before reaching $T = 8195 \times T_{DCLK}$ stops the debounce counter.

While the debounce counter is running, the bit CLK_ON in control register 3 is set to 1.

The interrupt is deleted after reading the status register or executes the command Delete_IRQ.

If pin N_PWR_ON is not used, it can be left open because of an internal pull-up resistor (typically 50 kΩ).

Figure 12-3. Timing Flow Pin N_PWR_ON, Status Bit N_Power_On



12.5 Pin PWR_ON

To switch the transceiver from OFF to IDLE mode, pin PWR_ON must set to 1 (minimum $0.8 \times V_{VSINT}$) for at least T_{PWR_ON} (see Figure 12-4 on page 46). The transceiver recognizes the positive edge and switches on DVCC and AVCC.

If V_{DVCC} exceeds 1.6V (typically) and the XTO is settled, the digital control logic is active and sets the status bit Power_On to 1, an interrupt is issued ($T_{PWR_ON_IRQ_1}$) and the output clock on pin CLK is available.

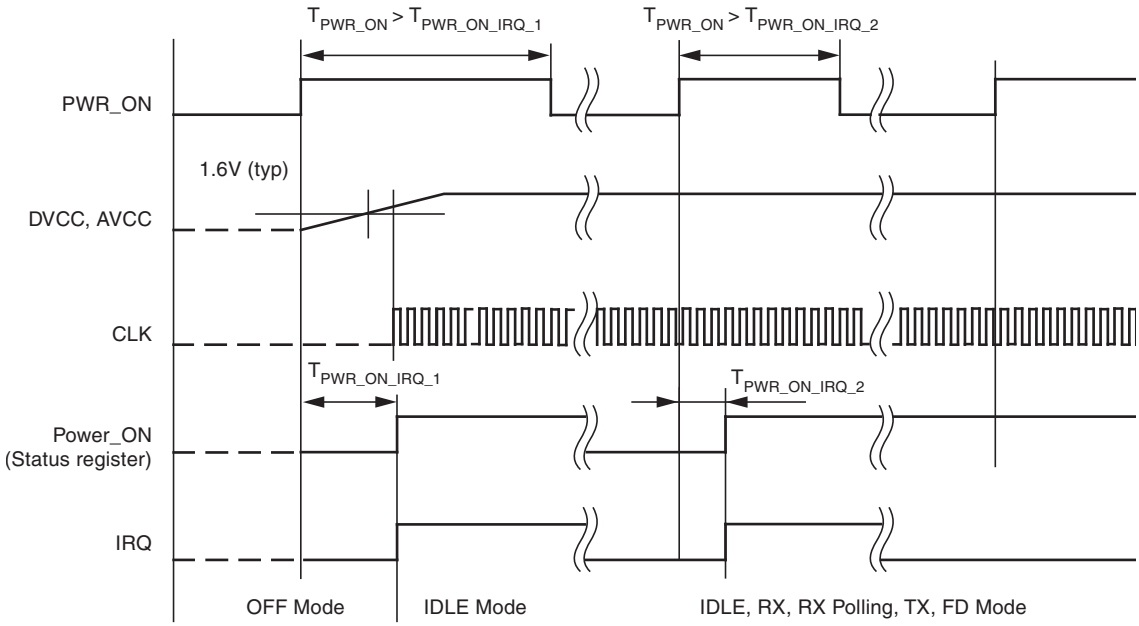
If the level on pin PWR_ON was set to 0 before the interrupt is issued, the transceiver stays in OFF mode.

If the transceiver is in any of the active modes (IDLE, RX, RX_Polling, TX, FD), a positive edge on pin PWR_ON sets Power_On to 1 (after $T_{PWR_ON_IRQ_2}$). The state transition Power_On 0 →1 generates an interrupt. If Power_On is still 1 during the positive edge on pin PWR_ON, no interrupt is issued. Power_On and the interrupt is deleted after reading the status register.

During Power_On = 1, the bit CLK_EN in control register 3 is set to 1.

Note: It is not possible to set the transceiver to OFF mode by setting pin PWR_ON to 0. If pin PWR_ON is not used, it must be connected to GND.

Figure 12-4. Timing Pin PWR_ON, Status Bit Power_On

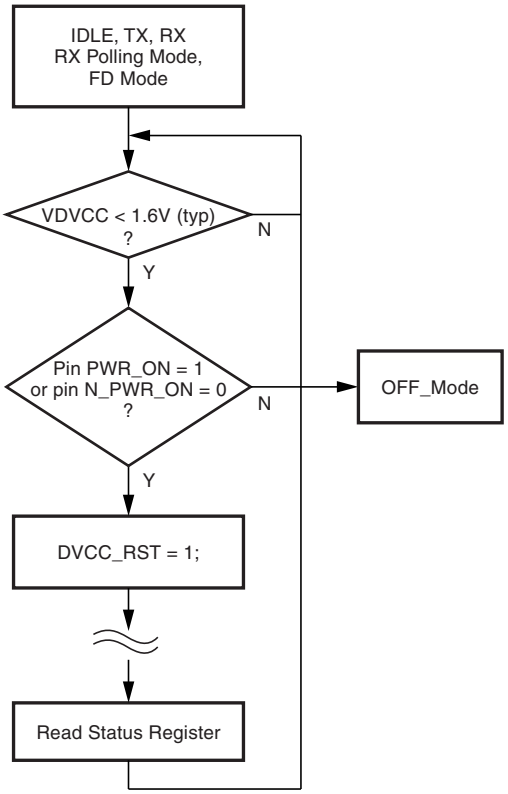


12.6 DVCC_RST

The status bit DVCC_RST is set to 1 if the voltage on pin DVCC V_{DVCC} drops under 1.6V (typically).

DVCC_RST is set to 0 if V_{DVCC} exceeds 1.6V (typically) and the status register is read via the 4-wire serial interface (see Figure 10-3 on page 34).

Figure 12-5. Timing Flow Status Bit DVCC_RST



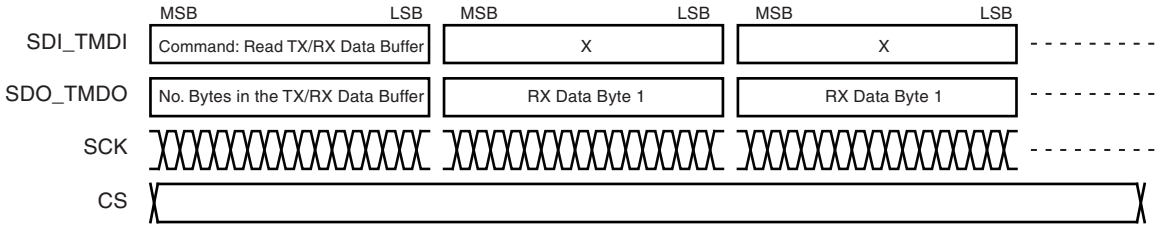
13. Transceiver Configuration

The configuration of the transceiver takes place via a 4-wire serial interface (CS, SCK, SDI_TMDI, SDO_TMDO) and is organized in 8-bit units. The configuration is initiated with a 8-bit command. While shifting the command into pin SDI_TMDI, the number of bytes in the TX/RX data buffer are available on pin SDO_TMDO. The read and write commands are followed by one or more 8-bit data units. Each 8-bit data transmission begins with the MSB.

13.1 Command: Read TX/RX Data Buffer

During a RX operation the user can read the received bytes in the TX/RX data buffer successively.

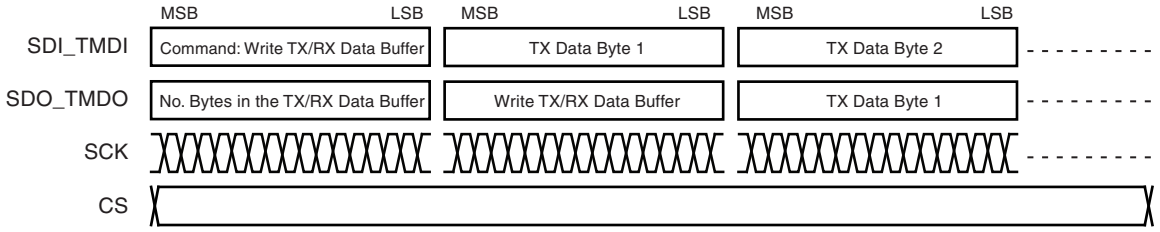
Figure 13-1. Read TX/RX Data Buffer



13.2 Command: Write TX/RX Data Buffer

During a TX operation the user can write the bytes in the TX/RX data buffer successively.

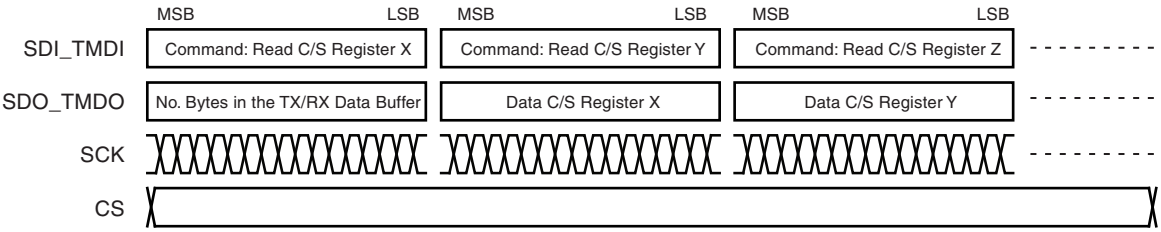
Figure 13-2. Write TX/RX Data Buffer



13.3 Command: Read Control/Status Register

The control and status registers can be read individually or successively.

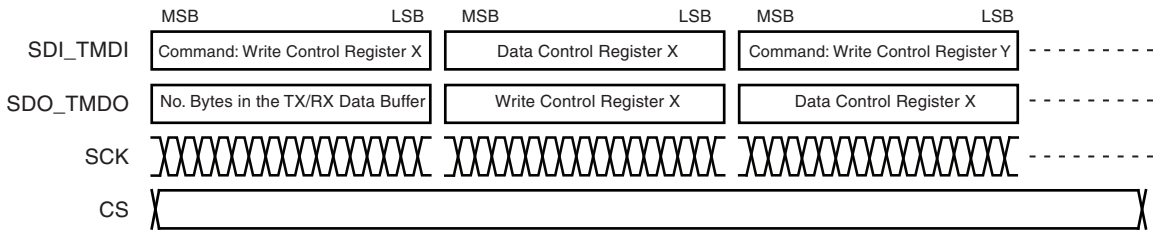
Figure 13-3. Read Control/Status Register



13.4 Command: Write Control Register

The control registers can be written individually or successively.

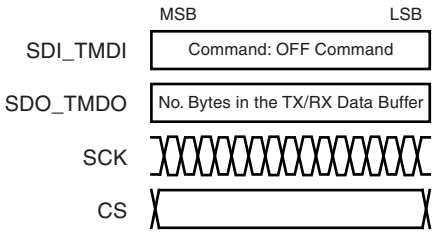
Figure 13-4. Write Control Register



13.5 Command: OFF Command

If the input level on pin PWR_ON is low and on the key input N_PWR_ON is high, the OFF command sets the transceiver to the OFF mode.

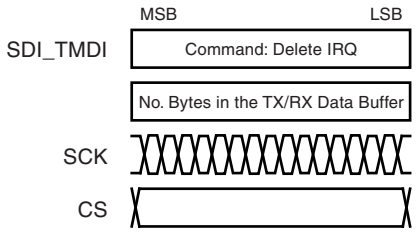
Figure 13-5. OFF Command



13.6 Command: Delete IRQ

The delete IRQ command sets pin IRQ to low.

Figure 13-6. Delete IRQ



13.7 Command Structure

The three most significant bits of the command (bit 5 to bit 7) indicates the command type. Bit 0 to bit 4 describes the target address when reading or writing to a control or status register.

Bit 0 to bit 4 in the command Write TX/RX Data Buffer defines the value N ($0 \leq N \leq 16$). The TX operation only will be started if the number of bytes in the TX buffer $\geq$ N. This function makes sure that the datastream will be sent without gaps. The TX operation only will be started if at least 1 byte are in the TX buffer. This means that N = 0 and N = 1 have the same function.

In all other commands Bit 0 to Bit 4 have no effect and should be set to 0 for compatibility reasons with future products.

Table 13-1. Command Structure

Command	MSB Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB Bit 0
Read TX/RX data buffer	0	0	0	X	X	X	X	X
Write TX/RX data buffer	0	0	1	N4	N3	N2	N1	N0
Read control/status register	0	1	0	A4	A3	A2	A1	A0
Write control register	0	1	1	A4	A3	A2	A1	A0
OFF command	1	0	0	X	X	X	X	X
Delete IRQ	1	0	1	X	X	X	X	X
Not used	1	1	0	X	X	X	X	X
Not used	1	1	1	X	X	X	X	X

13.8 4-wire Serial Interface

The 4-wire serial interface consists of the Chip Select (CS), the Serial Clock (SCK), the Serial Data Input (SDI_TMDI) and the Serial Data Output (SDO_TMDO). Data is transmitted/received bit by bit in synchronization with the serial clock.

Pin CS_POL defines the active level of the CS:

Table 13-2. Active Level of the CS

CS_POL	Function
0	CS active high
1	CS active low

When CS is inactive and the transceiver is not in RX transparent mode, SDO_TMDO is in a high-impedance state.

Pins SCK_POL and SCK_PHA defines the polarity and the phase of the serial clock SCK.

Figure 13-7. Serial Timing SCK_POL = 0, SCK_PHA = 0

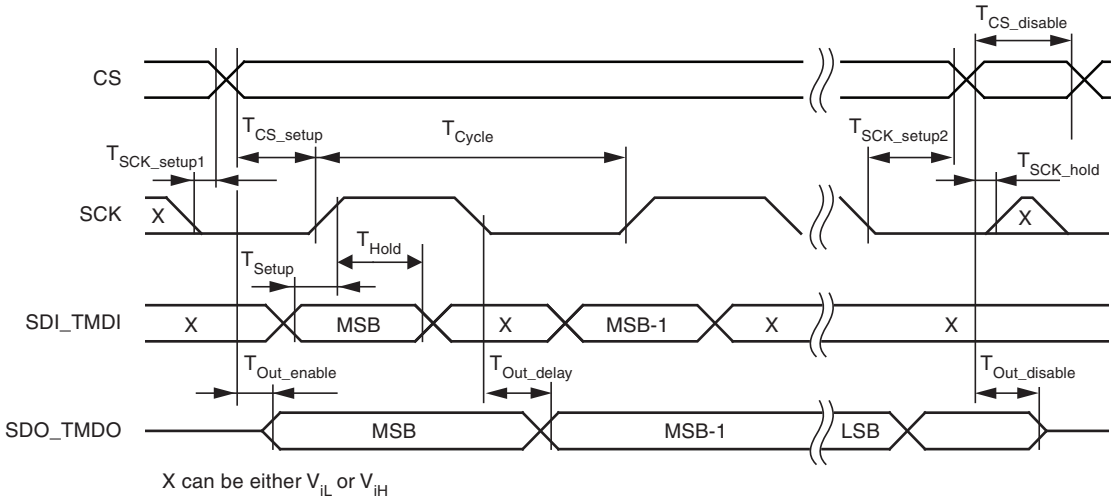


Figure 13-8. Serial Timing SCK_POL = 0, SCK_PHA = 1

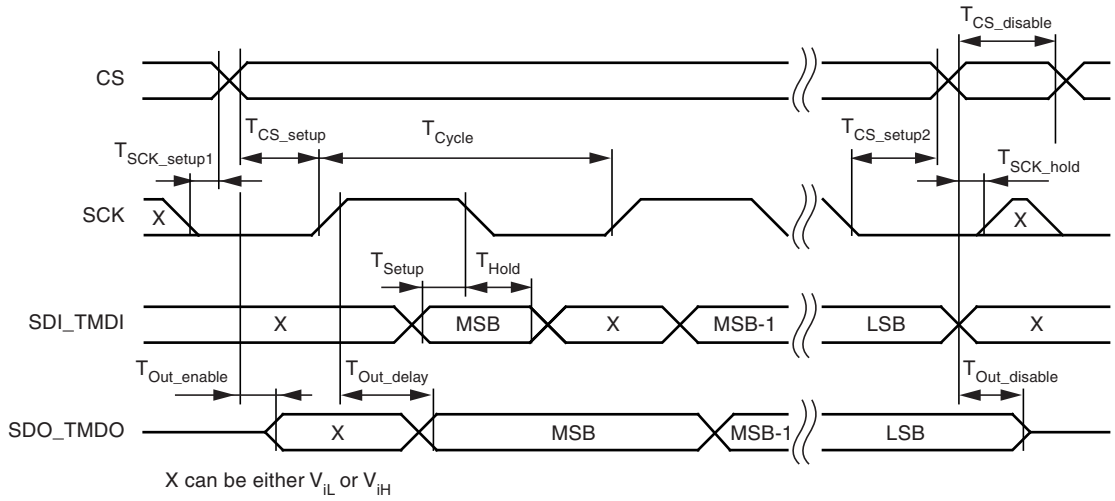


Figure 13-9. Serial Timing SCK_POL = 1, SCK_PHA = 0

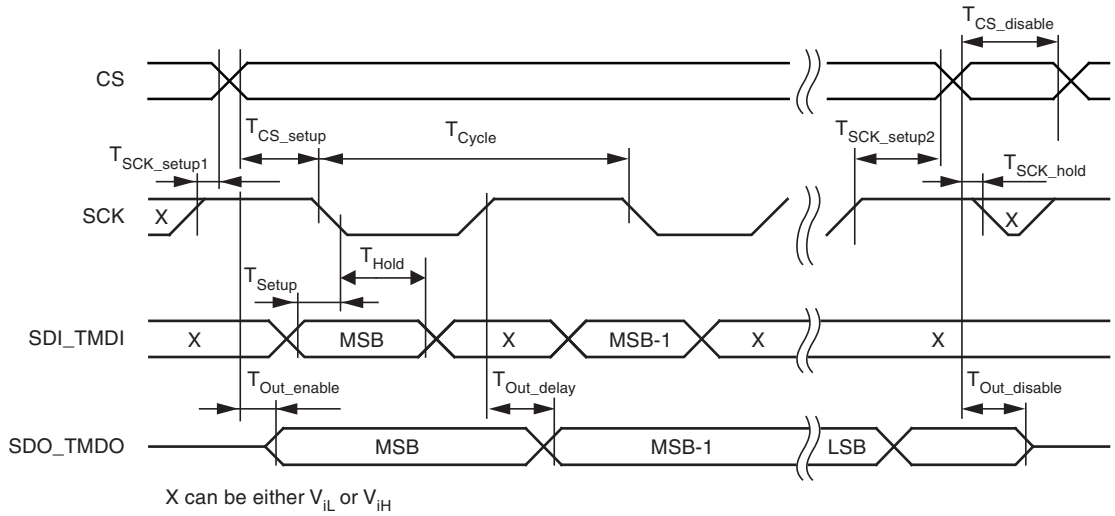
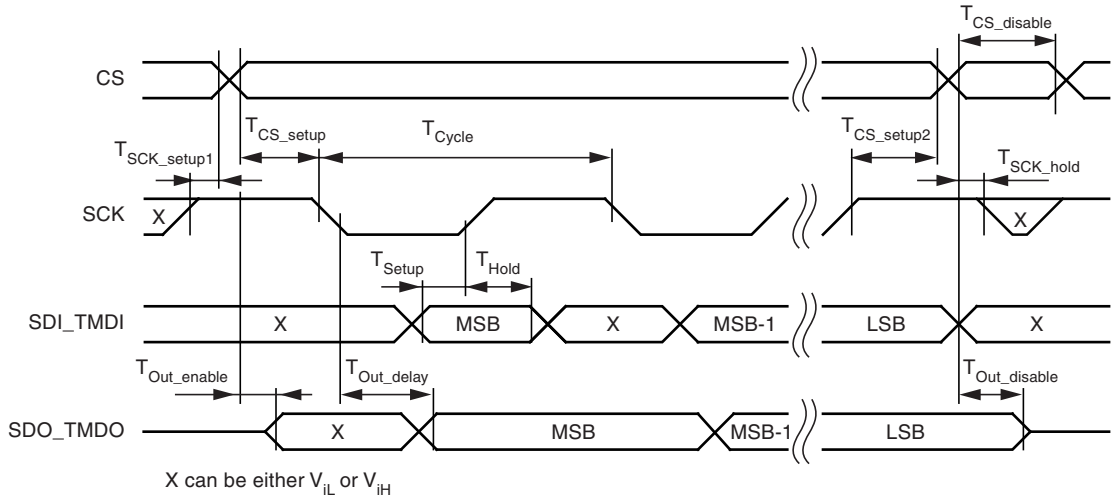


Figure 13-10. Serial Timing SCK_POL = 1, SCK_PHA = 1



14. Operation Modes

14.1 RX Operation

The transceiver is set to RX operation with the bits OPM0, OPM1 and OPM2 in control register 1

Table 14-1. Control Register 1

OPM2	OPM1	OPM0	Function
0	1	0	RX polling mode
0	1	1	RX mode

The transceiver is designed to consume less than 1 mA in RX operation while being sensitive to signals from a corresponding transmitter. This is achieved via the polling circuit. This circuits enable the signal path periodically for a short time. During this time the Bit-check logic verifies the presence of a valid transmitter signal. Only if a valid signal is detected the transceiver remains active and transfers the data to the connected microcontroller. This transfer take place either via the TX/RX data buffer or via the pin SDO_TMDO. If there is no valid signal present the transceiver is in sleep mode most of the time resulting in low current consumption. This condition is called RX polling mode. A connected microcontroller can be disabled during this time.

All relevant parameters of the polling logic can be configured by the connected microcontroller. This flexibility enables the user to meet the specifications in terms of current consumption, system response time, data rate etc.

In RX mode the RF transceiver is enabled permanently and the Bit-check logic verifies the presence of a valid transmitter signal. If a valid signal is detected the transceiver transfers the data to the connected microcontroller. This transfer takes place either via the TX/RX data buffer or via the pin SDO_TMDO.

14.1.1 RX Polling Mode

If the transceiver is in RX polling mode, it stays in a continuous cycle of three different modes. In sleep mode, the RF transceiver is disabled for the time period T_{Sleep} while consuming low current of $I_S = I_{IDLE_X}$. During the start-up period, $T_{Startup_PLL}$ and $T_{Startup_Sig_Proc}$, all signal processing circuits are enabled and settled. In the following Bit-check mode, the incoming data stream is analyzed bit by bit versus a valid transmitter signal. If no valid signal is present, the transceiver is set back to sleep mode after the period $T_{Bit\text{-}check}$. This period varies check by check as it is a statistical process. An average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. During $T_{Startup_PLL}$ the current consumption is $I_S = I_{RX_X}$. During $T_{Startup_Sig_Proc}$ and $T_{Bit\text{-}check}$ the current consumption is $I_S = I_{Startup_Sig_Proc_X}$. The condition of the transceiver is indicated on pin RX_ACTIVE (see Figure 14-1). The average current consumption in RX polling mode I_{Poll} is different in battery application or car application. To calculate I_{Poll} the index X must be replaced by VS1,2 in battery application or VS2 in car application (see section “Electrical Characteristics: General” on page 72).

$$I_{Poll} = \frac{I_{IDLE_X} \times T_{Sleep} + I_{Startup_PLL_X} \times T_{Startup_PLL} + I_{RX_X} \times (T_{Startup_Sig_Proc} + T_{Bitcheck})}{T_{Sleep} + T_{Startup_PLL} + T_{Startup_Sig_Proc} + T_{Bitcheck}}$$

To save current it is recommended CLK be disabled during RX polling mode. I_P does not include the current of the Microcontroller_Interface I_{VSINT}. If CLK is enabled during the RX polling mode the current consumption is calculated as follows:

$$I_{S_Poll} = I_{Poll} + I_{VSINT}$$

During T_{Sleep}, $T_{Startup_PLL}$ and $T_{Startup_Sig_Proc}$ the transceiver is not sensitive to a transmitter signals. To guarantee the reception of a transmitted command the transmitter must start the telegram with an adequate preburst. The required length of the preburst $T_{Preburst}$ depends on the polling parameters T_{Sleep}, $T_{Startup_PLL}$, $T_{Startup_Sig_Proc}$ and $T_{Bit\text{-}check}$. Thus, $T_{Bit\text{-}check}$ depends on the actual bit rate and the number of bits ($N_{Bit\text{-}check}$) to be tested.

$$T_{Preburst} \geq T_{Sleep} + T_{Startup_PLL} + T_{Startup_Sig_Proc} + T_{Bitcheck}$$

14.1.2 Sleep Mode

The length of period T_{Sleep} is defined by the 5-bit word sleep in control register 4, the extension factor X_{Sleep} defined by the bit X_{Sleep} in control register 4 and the basic clock cycle T_{DCLK}. It is calculated to be:

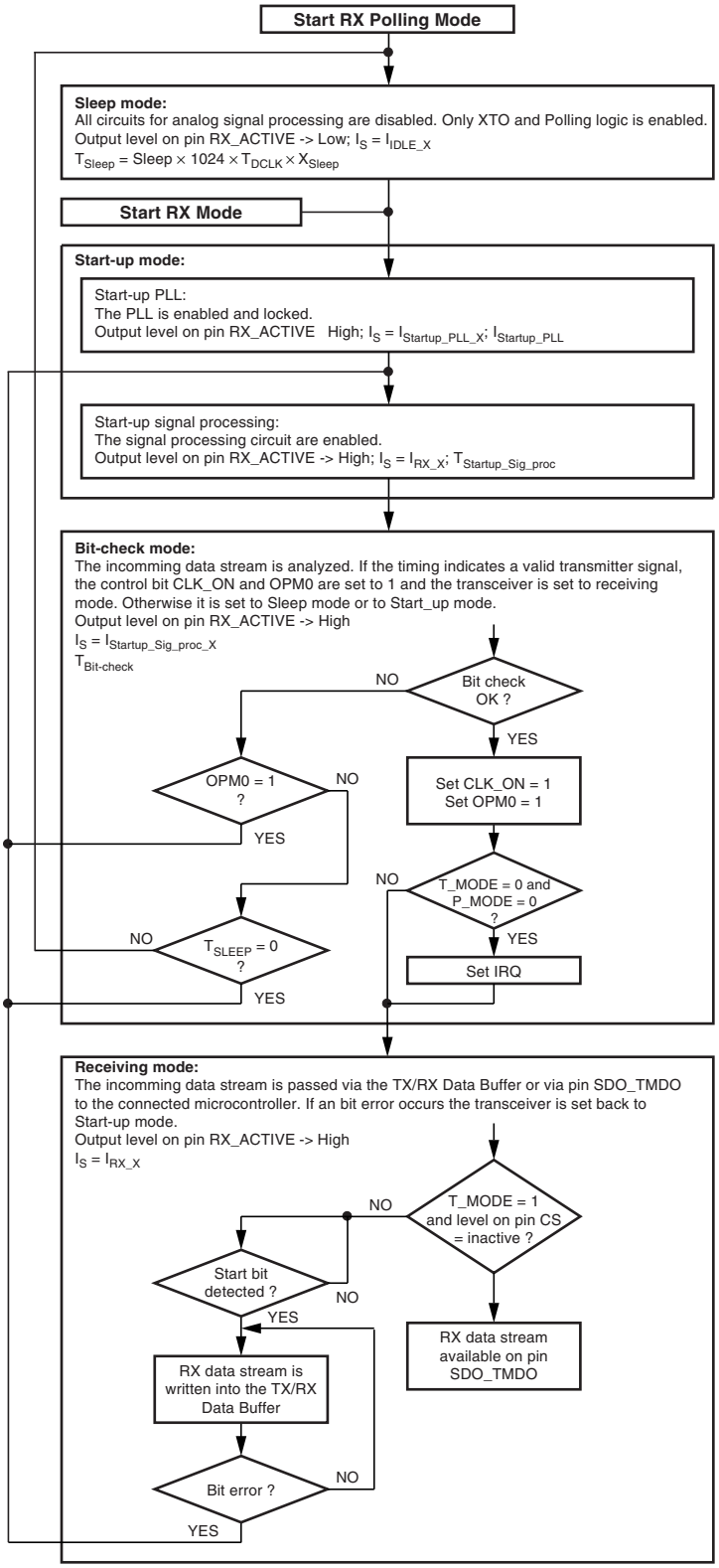
$$T_{Sleep} = Sleep \times 1024 \times T_{DCLK} \times X_{Sleep}$$

In US and European applications, the maximum value of T_{Sleep} is about 38 ms if X_{Sleep} is set to 1 (which is done by setting the bit X_{Sleep} in control register 4 to 0). The time resolution is about 1.2 ms in that case. The sleep time can be extended to about 300 ms by setting X_{Sleep} to 8 (which is done by setting X_{Sleep} in control register 4 to 1), the time resolution is then about 9.6 ms.

14.1.3 Start-up Mode

During $T_{Startup_PLL}$ the PLL is enabled and starts up. If the PLL is locked, the signal processing circuit starts up ($T_{Startup_Sig_Proc}$). After the start-up time all circuits are in stable condition and ready to receive.

Figure 14-1. Flow Chart RX Polling Mode/RX Mode



Sleep: Defined by bits Sleep 0 to Sleep 4 in Control Register 4

X_{Sleep}: Defined by bit XSleep in Control Register 4

T_{DCLK}: Basic clock cycle

$T_{Startup_PLL}$: $798.5 \times T_{DCLK}$ (typ)

$T_{Startup_Sig_Proc}$:

$930 \times T_{DCLK}$	(BR_Range 0)
$546 \times T_{DCLK}$	(BR_Range 1)
$354 \times T_{DCLK}$	(BR_Range 2)
$258 \times T_{DCLK}$	(BR_Range 3)

Is defined by the selected baud rate range and T_{DCLK} .The bit-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

$T_{Bit\text{-}check}$: Depends on the result of the bit check.

If the bit check is ok, $T_{Bit\text{-}check}$ depends on the number of bits to be checked ($N_{Bit\text{-}check}$) and on the utilized data rate.

If the bit check fails, the average time period for that check despends on the selected bit-rate range and on T_{XDCLK}. The bit-rate range is defined by bit Baud 0 and Baud 1 in Control Register 6.

If the transparent mode is not active and the transceiver detects a bit errror after a successful bit check and before the start bit is detected pin IRQ will be set to high and the transceiver is set back to start-up mode.

14.1.4 Bit-check Mode

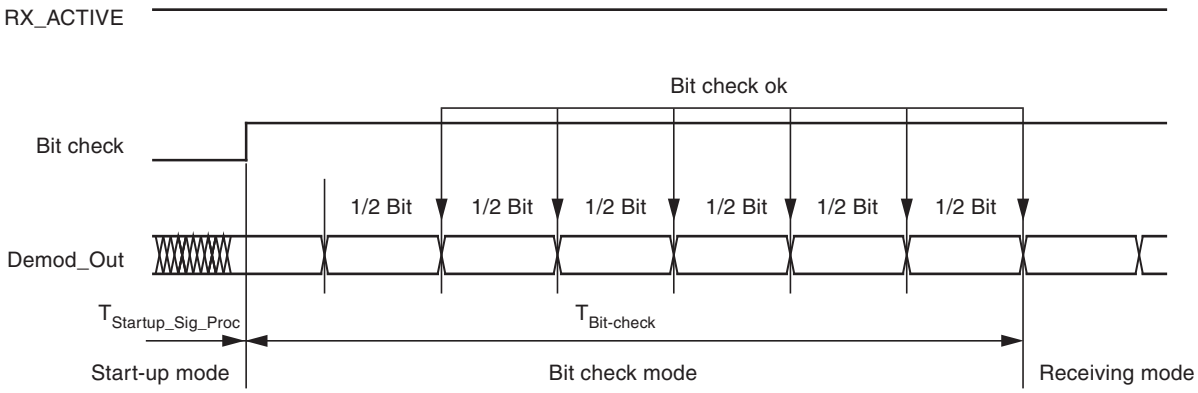
In Bit-check mode the incoming data stream is examined to distinguish between a valid signal from a corresponding transmitter and signals due to noise. This is done by subsequent time frame checks where the distance between 2 signal edges are continuously compared to a programmable time window. The maximum count of this edge to edge test before the transceiver switches to receiving mode is also programmable.

14.1.5 Bit-check Configuration

Assuming a modulation scheme that contains 2 edges per bit, two time frame checks are verifying one bit. This is valid for Manchester, Bi-phase and most other modulation schemes. The maximum count of bits to be checked can be set to 0, 3, 6 or 9 bits via the variable $N_{Bit\text{-}check}$ in control register 5. This implies 0, 6, 12 and 18 edge to edge checks respectively. If $N_{Bit\text{-}check}$ is set to a higher value, the transceiver is less likely to switch to receiving mode due to noise. In the presence of a valid transmitter signal, the Bit-check takes less time if $N_{Bit\text{-}check}$ is set to a lower value. In RX polling mode, the Bit-check time is not dependent on $N_{Bit\text{-}check}$ if no valid signal is present. Figure 14-2 shows an example where 3 bits are tested successful.

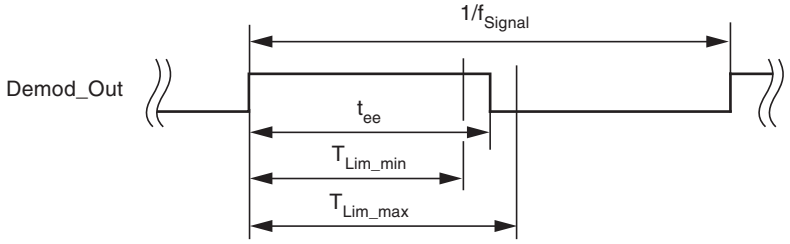
Figure 14-2. Timing Diagram for Complete Successful Bit-check

(Number of checked bits: 3)



According to Figure 14-3, the time window for the Bit-check is defined by two separate time limits. If the edge to edge time t_{ee} is in between the lower Bit-check limit T_{Lim_min} and the upper Bit-check limit T_{Lim_max}, the check will be continued. If t_{ee} is smaller than limit T_{Lim_min} or exceeds T_{Lim_max}, the Bit-check will be terminated and the transceiver switches to sleep mode.

Figure 14-3. Valid Time Window for Bit-check



For the best noise immunity it is recommended to use a low span between T_{Lim_min} and T_{Lim_max}. This is achieved using a fixed frequency at a 50% duty cycle for the transmitter preburst. A “11111...” or a “10101...” sequence in Manchester or bi-phase is a good choice concerning that advice. A good compromise between sensitivity and susceptibility to noise regarding the expected edge to edge time t_{ee} is a time window of ±38%. To get the maximum sensitivity the time window should be ±50% and then $N_{Bit\text{-}check} \geq 6$. Using preburst patterns that contain various edge to edge time periods, the Bit-check limits must be programmed according to the required span.

The Bit-check limits are determined by means of the formula below:

$$T_{Lim_min} = Lim_min \times T_{XDCLK}$$
$$T_{Lim_max} = (Lim_max\ -1) \times T_{XDCLK}$$

Lim_min is defined by the bits Lim_min 0 to Lim_min 5 in control register 5.
Lim_max is defined by the bits Lim_max 0 to Lim_max 5 in control register 6.

Using the above formulas, Lim_min and Lim_max can be determined according to the required T_{Lim_min}, T_{Lim_max} and T_{XDCLK}. The time resolution defining T_{Lim_min} and T_{Lim_max} is T_{XDCLK}. The minimum edge to edge time t_{ee} is defined according to the section “Receiving Mode” on page 58. The lower limit should be set to Lim_min ≥ 10. The maximum value of the upper limit is Lim_max = 63.

Figure 14-4, Figure 14-5 and Figure 14-6 on page 57 illustrate the Bit-check for the Bit-check limits Lim_min = 14 and Lim_max = 24. The signal processing circuits are enabled during $T_{Startup_PLL}$ and $T_{Startup_Sig_Proc}$. The output of the ASK/FSK demodulator (Demod_Out) is undefined during that period. When the Bit-check becomes active, the Bit-check counter is clocked with the cycle T_{XDCLK}.

Figure 14-4 shows how the Bit-check proceeds if the Bit-check counter value CV_Lim is within the limits defined by Lim_min and Lim_max at the occurrence of a signal edge. In Figure 14-5 on page 57 the Bit-check fails as the value CV_Lim is lower than the limit Lim_min. The Bit-check also fails if CV_Lim reaches Lim_max. This is illustrated in Figure 14-6 on page 57.

Figure 14-4. Timing Diagram During Bit-check

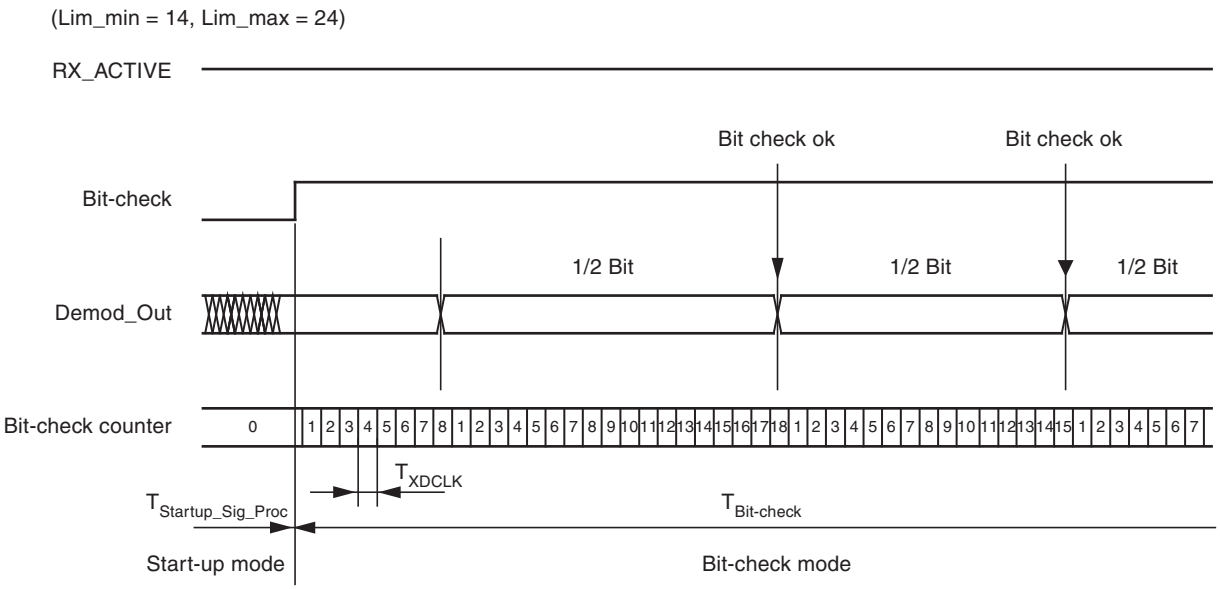


Figure 14-5. Timing Diagram for Failed Bit-check (Condition CV_Lim < Lim_min)

(Lim_min = 14, Lim_max = 24)

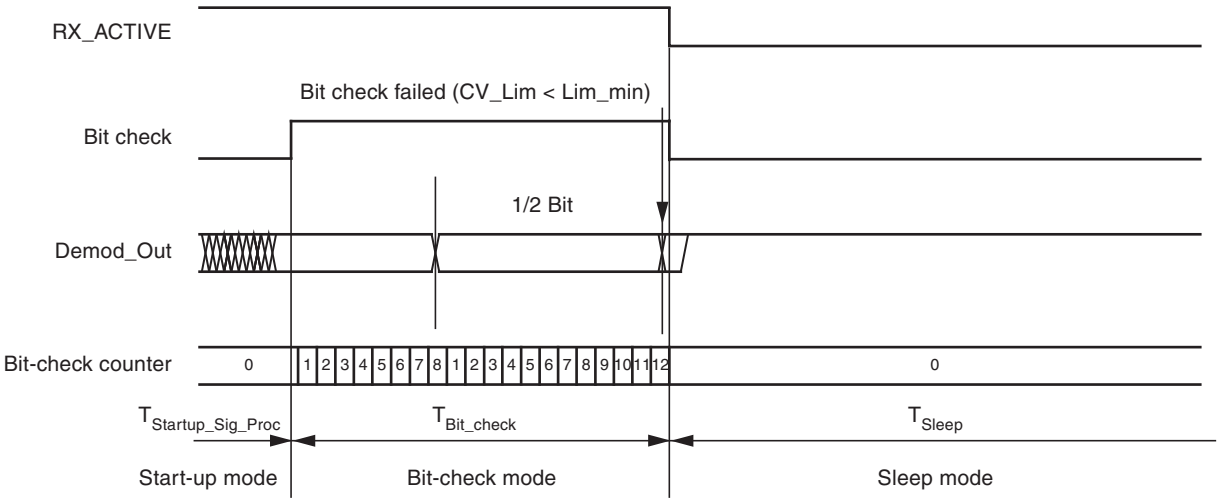
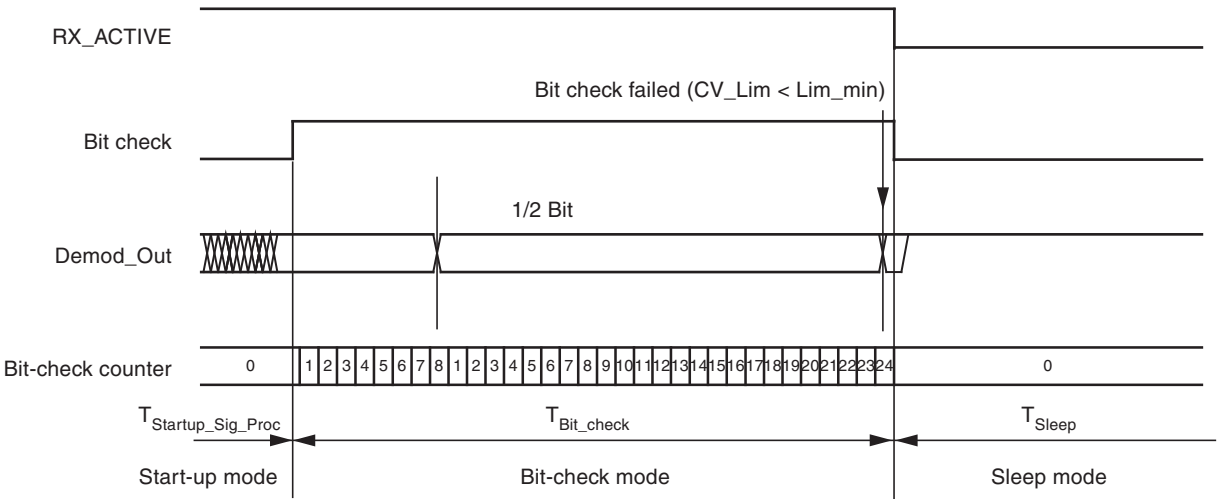


Figure 14-6. Timing Diagram for Failed Bit-check (Condition: CV_Lim ≥ Lim_max)

(Lim_min = 14, Lim_max = 24)



14.1.6 Duration of the Bit-check

If no transmitter is present during the Bit-check, the output of the ASK/FSK demodulator delivers random signals. The Bit-check is a statistical process and $T_{Bit\text{-}check}$ varies for each check. Therefore, an average value for $T_{Bit\text{-}check}$ is given in the electrical characteristics. $T_{Bit\text{-}check}$ depends on the selected bit-rate range and on T_{XDCLK}. A higher bit-rate range causes a lower value for $T_{Bit\text{-}check}$ resulting in a lower current consumption in RX polling mode.

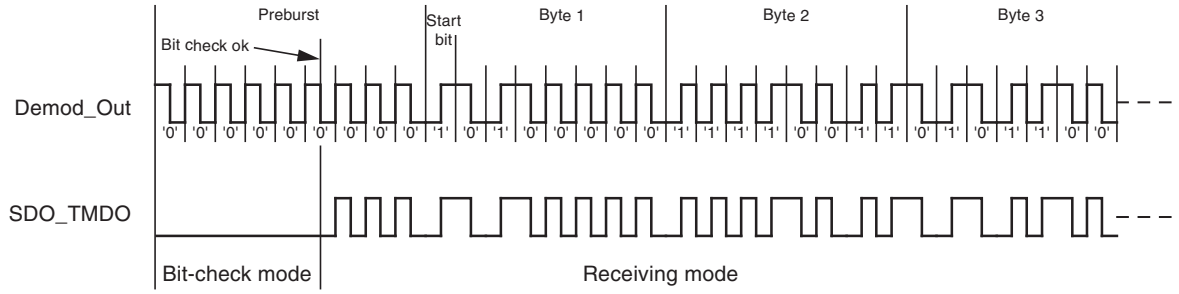
In the presence of a valid transmitter signal, $T_{Bit\text{-}check}$ is dependent on the frequency of that signal, f_{Signal}, and the count of the bits, $N_{Bit\text{-}check}$. A higher value for $N_{Bit\text{-}check}$ thereby results in a longer period for $T_{Bit\text{-}check}$ requiring a higher value for the transmitter pre-burst $T_{Preburst}$.

14.1.7 Receiving Mode

If the Bit-check was successful for all bits specified by $N_{Bit\text{-}check}$, the transceiver switches to receiving mode. To activate a connected microcontroller, bit CLK_ON in control register 3 is set to 1. An interrupt is issued at pin IRQ if the control bits T_MODE = 0 and P_MODE = 0.

If the transparent mode is active (T_MODE = 1) and the level on pin CS is inactive (no data transfer via the serial interface), the RX data stream is available on pin SDO_TMDO (Figure 14-7).

Figure 14-7. Receiving Mode (TMODE = 1)



If the transparent mode is inactive (T_MODE = 0), the received data stream is buffered in the TX/RX data buffer (see Figure 14-8 on page 59). The TX/RX data buffer is only usable for Manchester and Bi-phase coded signals. It is permanently possible to transfer the data from the data buffer via the 4-wire serial interface to a microcontroller (see Figure 13-1 on page 47).

Buffering of the data stream:
After a successful Bit-check, the transceiver switches from Bit-check mode to receiving mode. In receiving mode the TX/RX data buffer control logic is active and examines the incoming data stream. This is done, like in the Bit-check, by subsequent time frame checks where the distance between two edges is continuously compared to a programmable time window as illustrated in Figure 14-8 on page 59. Only two distances between two edges in Manchester and Bi-phase coded signals are valid (T and 2T).

The limits for T are the same as used for the Bit-check. They can be programmed in control register 5 and 6 (Lim_min, Lim_max).

The limits for 2T are calculated as follows:
Lower limit of 2T:

$$Lim_min_2T = (Lim_min + Lim_max) - (Lim_max - Lim_min) / 2 \quad T_{Lim_min_2T} = Lim_min_2T \times T_{XDCLK}$$

Upper limit of 2T:

$$Lim_max_2T = (Lim_min + Lim_max) + (Lim_max - Lim_min) / 2$$

$$T_{Lim_max_2T} = (Lim_max_2T - 1) \times T_{XDCLK}$$

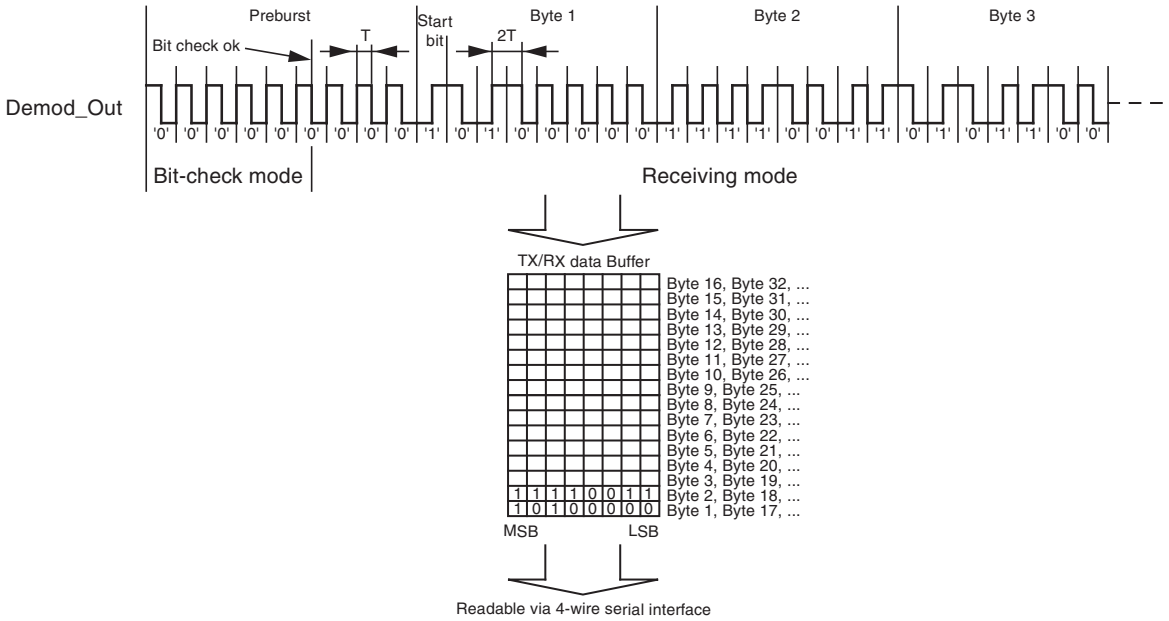
If the result of Lim_min_2T or Lim_max_2T is not an integer value, it will be round up.

If the TX/RX data buffer control logic detects the start bit, the data stream is written in the TX/RX data buffer byte by byte. The start bit is part of the first data byte and must be different from the bits of the preburst. If the preburst consists of a sequence of “00000...”, the start bit must be a 1. If the preburst consists of a sequence of “11111...”, the start bit must be a 0.

If the data stream consists of more than 16 bytes, a buffer overflow occurs and the TX/RX data buffer control logic overwrites the bytes already stored in the TX/RX data buffer. So it is very important to ensure that the data is read in time so that no buffer overflow occurs in that case (see Figure 13-1 on page 47). There is a counter that indicates the number of received bytes in the TX/RX data buffer (see section "Transceiver Configuration" on page 47). If a byte is transferred to the microcontroller, the counter is decremented, if a byte is received, the counter is incremented. The counter value is available via the 4-wire serial interface.

An interrupt is issued if the counter while counting forwards reaches the value defined by the control bits IR0 and IR1 in control register 1.

Figure 14-8. Receiving Mode (TMODE = 0)



If the TX/RX data buffer control logic detects a bit error, an interrupt is issued and the transceiver is set back to the start-up mode (see Figure 14-1 on page 54 and Figure 14-9).

Bit error: a) $t_{ee} < T_{Lim_min}$ or $T_{Lim_max} < t_{ee} < T_{Lim_min_2T}$ or $t_{ee} > T_{Lim_max_2T}$
b) Logical error (no edge detected in the bit center)

Note: The byte consisting of the bit error will not be stored in the TX/RX data buffer. Thus it is not available via the 4-wire serial interface.

Writing the control register 1, 4, 5, 6 or 7 during receiving mode resets the TX/RX data buffer control logic and the counter which indicates the number of received bytes. If the bits OPM0 and OPM1 are still 1 and OPM2 is still 0 after writing to a control register, the transceiver changes to the start-up mode (start-up signal processing).

Figure 14-9. Bit Error (TMODE = 0)

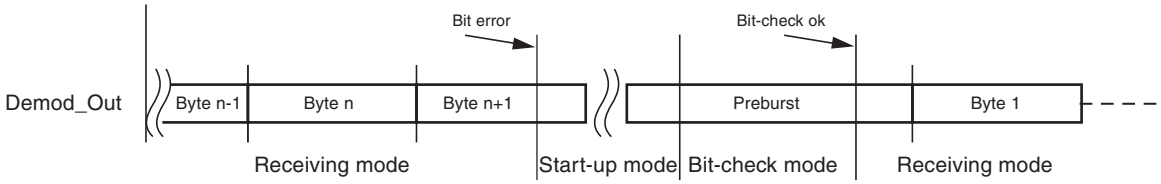


Table 14-2. RX Demodulation Scheme

Mode	ASK/_NFSK	T_MODE	RF_{IN}	Bit in TX/RX Data Buffer	Level on Pin SDO_TMDO
RX	0	0	$f_{FSK_L} \rightarrow f_{FSK_H}$	1	X
		0	$f_{FSK_H} \rightarrow f_{FSK_L}$	0	X
		1	f_{FSK_H}	-	1
		1	f_{FSK_L}	-	0
	1	0	f_{ASK} off $\rightarrow f_{ASK}$ on	1	X
		0	f_{ASK} on $\rightarrow f_{ASK}$ off	0	X
		1	f_{ASK} on	-	1
		1	f_{ASK} off	-	0

14.1.8 Recommended Lim_min and Lim_max for Maximum Sensitivity

The sensitivity measurement in the section "Low-IF Receiver" on page 10, in Table 7-3 and Table 7-4 on page 12 have been done with the Lim_min and Lim_max values according to Table 14-3. These values are optimized for maximum sensitivity. Note that since these Limits are optimized for sensitivity the number of checked bit $N_{Bit\text{-}check}$ has to be at least 6 to prevent the circuit from waking up too often in polling mode due to noise.

Table 14-3. Recommended Lim_min and Lim_max Values for Different Bit Rates

f_{RF} (f_{XTAL})/ MHz	1.0 Kbit/s BR_Range_0 XLim = 1	2.4 Kbit/s BR_Range_0 XLim = 0	5 Kbit/s BR_Range_1 XLim = 0	10 Kbit/s BR_Range_2 XLim = 0	20 Kbit/s BR_Range_3 XLim = 0
315 (12.73193)	Lim_min = 13 (251 µs) Lim_max = 38 (715 µs)	Lim_min = 12 (121 µs) Lim_max = 34 (332 µs)	Lim_min = 11 (55 µs) Lim_max = 32 (156 µs)	Lim_min = 11 (28 µs) Lim_max = 32 (78 µs)	Lim_min = 11 (14 µs) Lim_max = 32 (39 µs)
433.92 (13.25311)	Lim_min = 13 (251 µs) Lim_max = 38 (715 µs)	Lim_min = 11 (106 µs) Lim_max = 32 (299 µs)	Lim_min = 11 (53 µs) Lim_max = 32 (150 µs)	Lim_min = 11 (27 µs) Lim_max = 32 (75 µs)	Lim_min = 11 (13 µs) Lim_max = 32 (37 µs)
868.3 (13.41191)	Lim_min = 13 (248 µs) Lim_max = 38 (706 µs)	Lim_min = 12 (115 µs) Lim_max = 34 (315 µs)	Lim_min = 11 (52 µs) Lim_max = 32 (148 µs)	Lim_min = 11 (26 µs) Lim_max = 32 (74 µs)	Lim_min = 11 (13 µs) Lim_max = 32 (37 µs)

14.2 TX Operation

The transceiver is set to TX operation by using the bits OPM0, OPM1 and OPM2 in the control register 1.

Table 14-4. Control Register 1

OPM2	OPM1	OPM0	Function
0	0	1	TX mode

Before activating the TX mode, the TX parameters (bit rate, modulation scheme...) must be selected as illustrated in Figure 14-10 on page 62. The bit rate depends on Baud0 and Baud1 in control register 6 and TX0 to TX5 in control register 7 (see section "Control Register" on page 37). The modulation is selected with ASK_NFSK in control register 4. The FSK frequency deviation is fixed to about ±19 kHz (see Table 9-1 on page 30). If P_Mode is set to 1, the Manchester modulator is disabled and pattern mode is active (NRZ, see Table 14-5 on page 64).

After the transceiver is set to TX mode the start-up mode is active and the PLL is enabled. If the PLL is locked, the TX mode is active.

If the transceiver is in start-up or TX mode, the TX/RX data buffer can be loaded via the 4-wire serial interface. After N bytes are in the buffer and the TX mode is active, the transceiver starts transmitting automatically (beginning with the MSB). Bit 0 to Bit 4 in the command Write TX/RX Data Buffer defines the value N ($0 \leq N \leq 16$; see section "Command Structure" on page 49). While transmitting, it is permanently possible to load new data in the TX/RX data buffer. To prevent a buffer overflow or interruptions during transmitting the user must ensure that data is loaded at the same speed as it is transmitted.

There is a counter that indicates the number of bytes to be transmitted (see section "Transceiver Configuration" on page 47). If a byte is loaded, the counter is incremented, if a byte is transmitted, the counter is decremented. The counter value is available via the 4-wire serial interface. An IRQ is issued if the counter reaches the value defined by the control bits IR0 and IR1 in control register 1.

Note: Writing to the control register 1, 4, 5, 6 or 7 during TX mode, resets the TX/RX data buffer and the counter which indicates the number of bytes to be transmitted.

If T_Mode in control register 1 is set to 1, the transceiver is in TX transparent mode. In this mode the TX/RX data buffer is disabled and the TX data stream must be applied on pin SDI_TMDI. Figure 14-10 on page 62 illustrates the flow chart of the TX transparent mode.

Figure 14-10. TX Operation (T_MODE = 0)

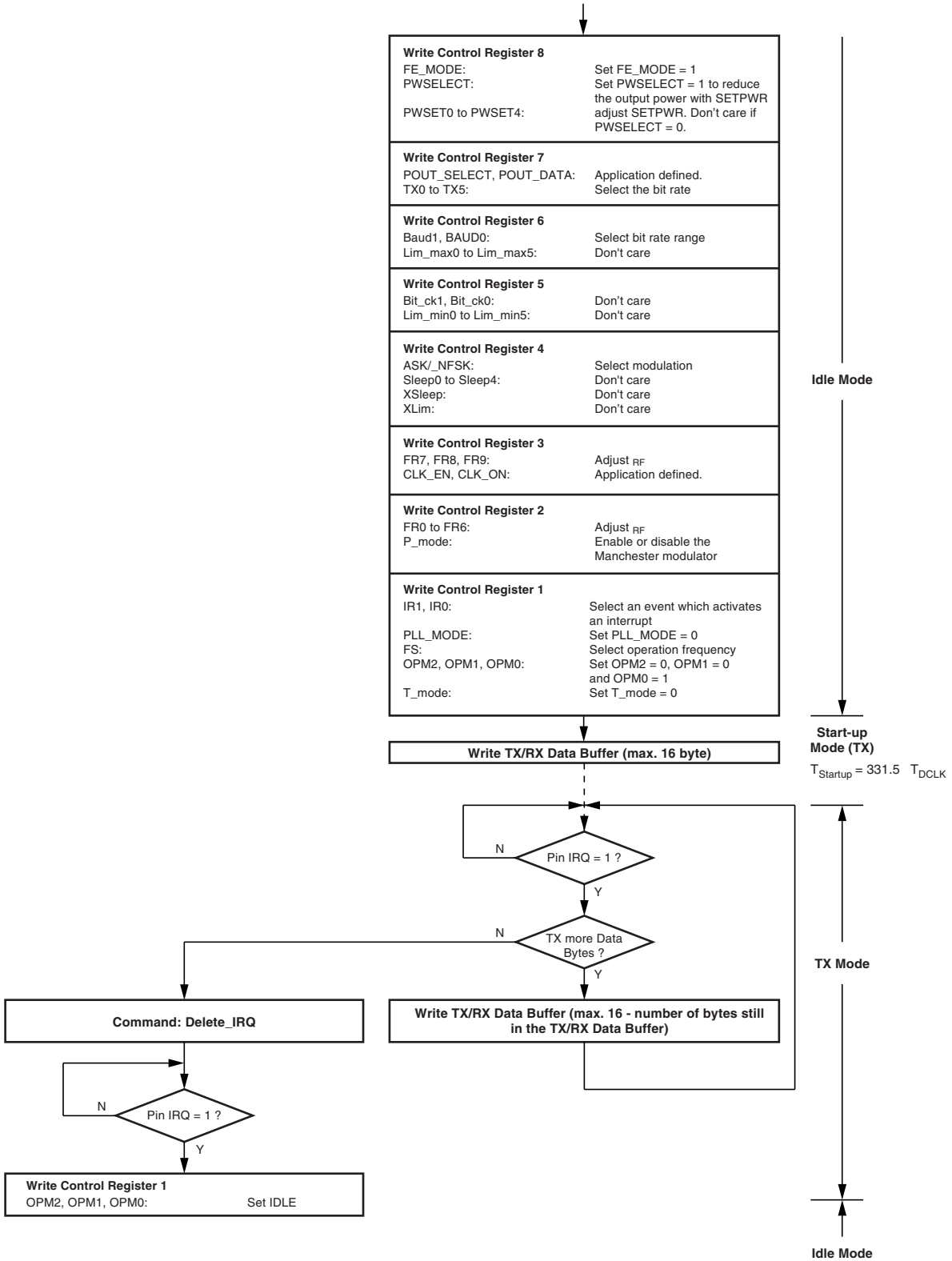


Figure 14-11. TX Transparent Mode (T_MODE = 1)

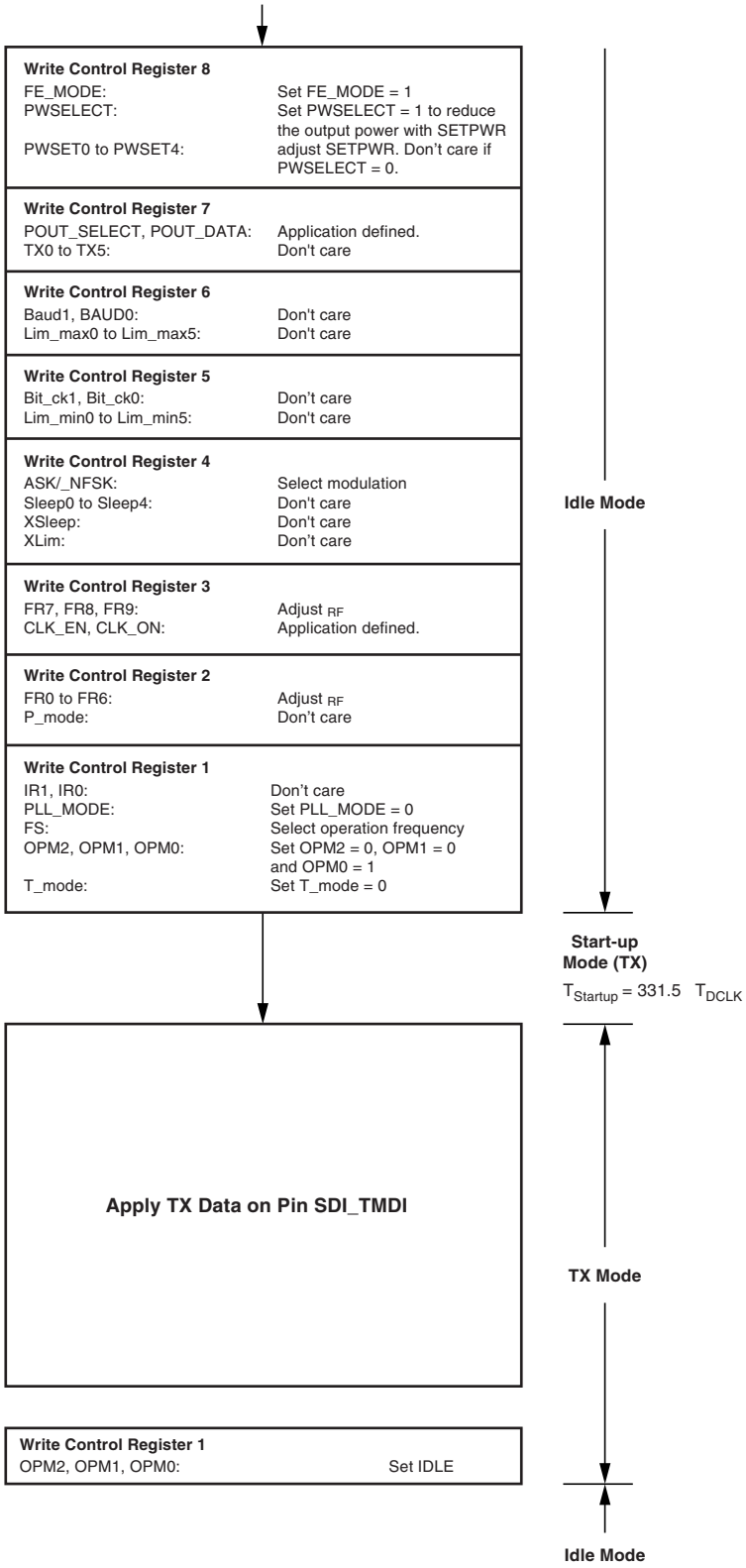


Table 14-5. TX Modulation Schemes

Mode	ASK/_NFSK	P_Mode	T_Mode	Bit in TX/RX Data Buffer	Level on Pin SDI_TMDI	RF_{OUT}
TX	0	0	0	1	X	$f_{FSK_L} \rightarrow f_{FSK_H}$
		0	0	0	X	$f_{FSK_H} \rightarrow f_{FSK_L}$
		1	0	1	X	f_{FSK_H}
		1	0	0	X	f_{FSK_L}
		X	1	X	1	f_{FSK_H}
		X	1	X	0	f_{FSK_L}
	1	0	0	1	X	f_{ASK} off $\rightarrow f_{ASK}$ on
		0	0	0	X	f_{ASK} on $\rightarrow f_{ASK}$ off
		1	0	1	X	f_{ASK} on
		1	0	0	X	f_{ASK} off
		X	1	X	1	f_{ASK} on
		X	1	X	0	f_{ASK} off

14.3 Full-duplex Operation

The transceiver is set to **f**ull-**d**uplex mode (FD mode) by using the bits OPM0, OPM1 and OPM2 in the control register 1. In FD mode 2 transceiver exchange the content of the TX buffer simultaneously. One transceiver must be configured as master and one as slave.

Table 14-6. Control Register 1

OPM2	OPM1	OPM0	Function
1	0	1	Full-duplex mode (Master)
1	1	1	Full-duplex mode (Slave)

Before activating FD mode in both transceivers, the bit rate must be selected in control register 6 (Baud1 = 0, Baud0 = 1). Additionally, in the slave the limits for the Bit-check and the number of bits to be checked during the Bit-check $N_{Bit\text{-}check}$ must be adjusted in control register 5 and 6 (Lim_min0 ... Lim_min5, Lim_max0 ... Lim_max5, BitChk0, BitChk1).

After activating the FD mode in control register 1, both transceivers are in the startup mode. During the startup mode, in master and slave, the TX data stream can be written in the TX buffer.

In the master the TX data stream consists of preburst, startbit, synchronization pattern (3 bytes) and maximally 8 bytes of data. The preburst contains a sequence of “11111...”. The minimum applicable preburst length is 15 bits and can be extended in 8 bit steps up to 95 bits. The value of the start bit is fixed and must be a 0. The position of the start bit is the LSB in the last byte of the preburst. The synchronization pattern contains 3 bytes with a fixed value (Byte1: FF hex, Byte2: 00 hex, Byte3: 00 hex). The data block is user defined and contains maximally 8 bytes. If the preburst contains more than 39 bits the area for the data block will be equally reduced (Figure 14-12 on page 65.)

In the slave the TX data stream consists of the synchronization pattern (3 bytes) and also maximally 8 bytes of data. The synchronization pattern contains 3 bytes with a fixed value (Byte1: 00 hex, Byte2: 7F hex, Byte3: FF hex). The data block is user defined and contains maximally 8 bytes (Figure 14-12 on page 65). The length of the data block must be equal in the master and slave.

If the time $T_{Startup\text{-}PLL\text{-}fd}$ (798.5 × T_{DCLK}) is elapsed the PLL is enabled and locked.

The master activates the power amplifier (PA) and starts transmitting the preburst, startbit, synchronization pattern and data block, when the PLL is locked and at least N bytes are in the TX Buffer. Bit 0 to bit 4 in the command Write TX/RX Data Buffer defines the value N ($0 \le N \le 16$; see section "Command Structure" on page 49).

If the PLL is locked, the slave activates the PA and enables the analog signal processing. After $T_{Startup\text{-}sig\text{-}proc\text{-}fd}$ (546 × T_{DCLK}) the analog signal processing is settled and the slave begins with the Bit-check. If the Bit-check was successful, the start bit was detected and at least N Bytes are in the TX Buffer, the slave starts transmitting the synchronization pattern and the data block.

While transmitting the synchronization pattern, a synchronization procedure synchronizes both transceivers. Thus master and slave are synchronized while transmitting the data block.

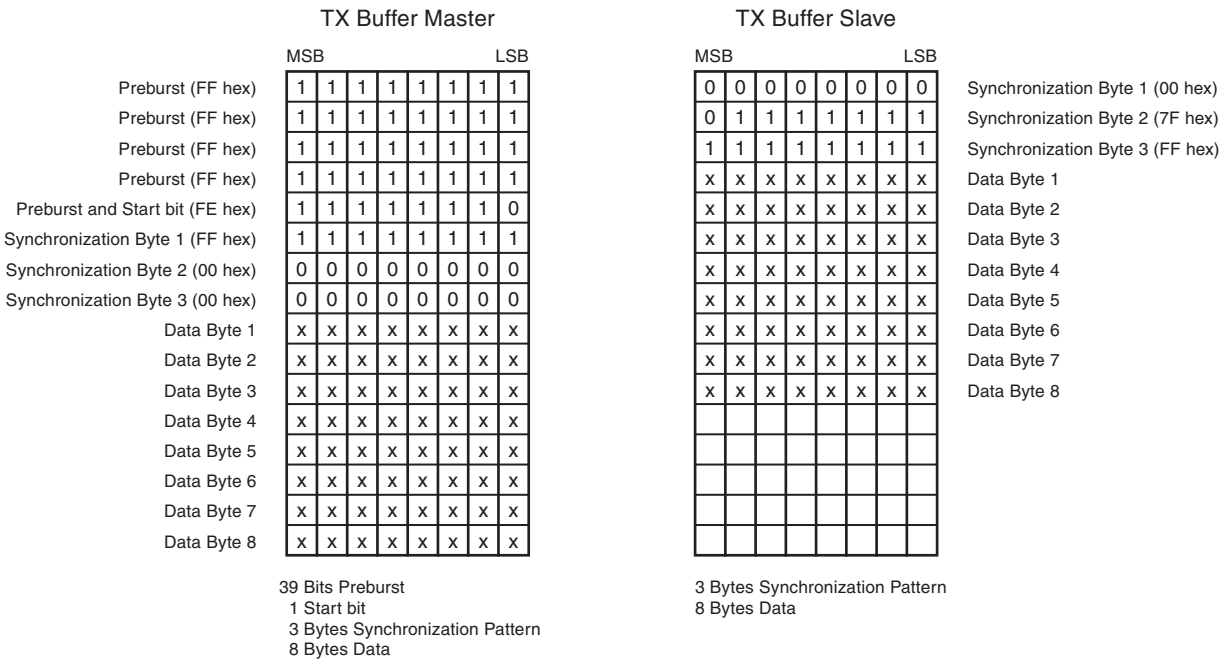
If the TX buffer is empty, an interrupt will be issued and the PA will be switched off after the time T_{Delay} (168 × T_{DCLK}). T_{Delay} is implemented because of different internal delays in the RX signal path in master and slave.

While transmitting the data block, the receiving data is EX-OR-ed with the transmitting data and the result is written in the RX Buffer. Thus, after the FD operation the TX data of the slave is in the RX buffer of the master and the TX data of the master is in the RX Buffer of the slave.

After recognizing the interrupt, the microcontroller can read out the received data from the TX/RX data buffer. During writing the command "Read TX/RX Data Buffer" the number of received bytes in the buffer is issued on pin SDO_TMDO.

After reading the TX/RX Data Buffer the transceiver should be set to the IDLE mode.

Figure 14-12. TX Buffer FD Mode



The timing of the FD mode is illustrated in Figure 14-13 on page 67. A proper data transfer takes place if the FD mode is enabled in the slave before it is enabled in the master. If the FD mode is enabled in the master before it is enabled in the slave, a maximum delay T_{FD_sync} is allowed for a proper operation. T_{FD_sync} depends on the preburst length and the number of bits to be checked during the Bit-check. This is calculated as follows:

$$T_{FD_sync} < T_{Preburst} - T_{Startup\text{-}sig\text{-}proc\text{-}fd} - T_{Bit\text{-}check\text{-}min}$$

Table 14-7. $T_{Bit\text{-}check\text{-}min}$

$N_{Bit\text{-}check}$	$T_{Bit\text{-}check\text{-}min}$
3	$4 \times 168 \times T_{DCLK}$
6 (recommended)	$7 \times 168 \times T_{DCLK}$
9	$10 \times 168 \times T_{DCLK}$

This means, to get a extended time period for enabling the FD mode, increase the preburst length in the master and reduce $N_{Bit\text{-}check}$ in the slave. The reference points for T_{FD_sync} are the sampling edge (pin SCK) for the LSB while writing control register 1.

For a proper operation in the slave, a wake-up due to noise must be prevent (bit check + start bit ok). To achieve this for the slave the following adjustments are recommended:

1. Set $N_{BIT\text{-}check} \geq 6$
2. Start FD mode in master and slave as simultaneously as possible.

Figure 14-13. Timing Full-duplex Mode

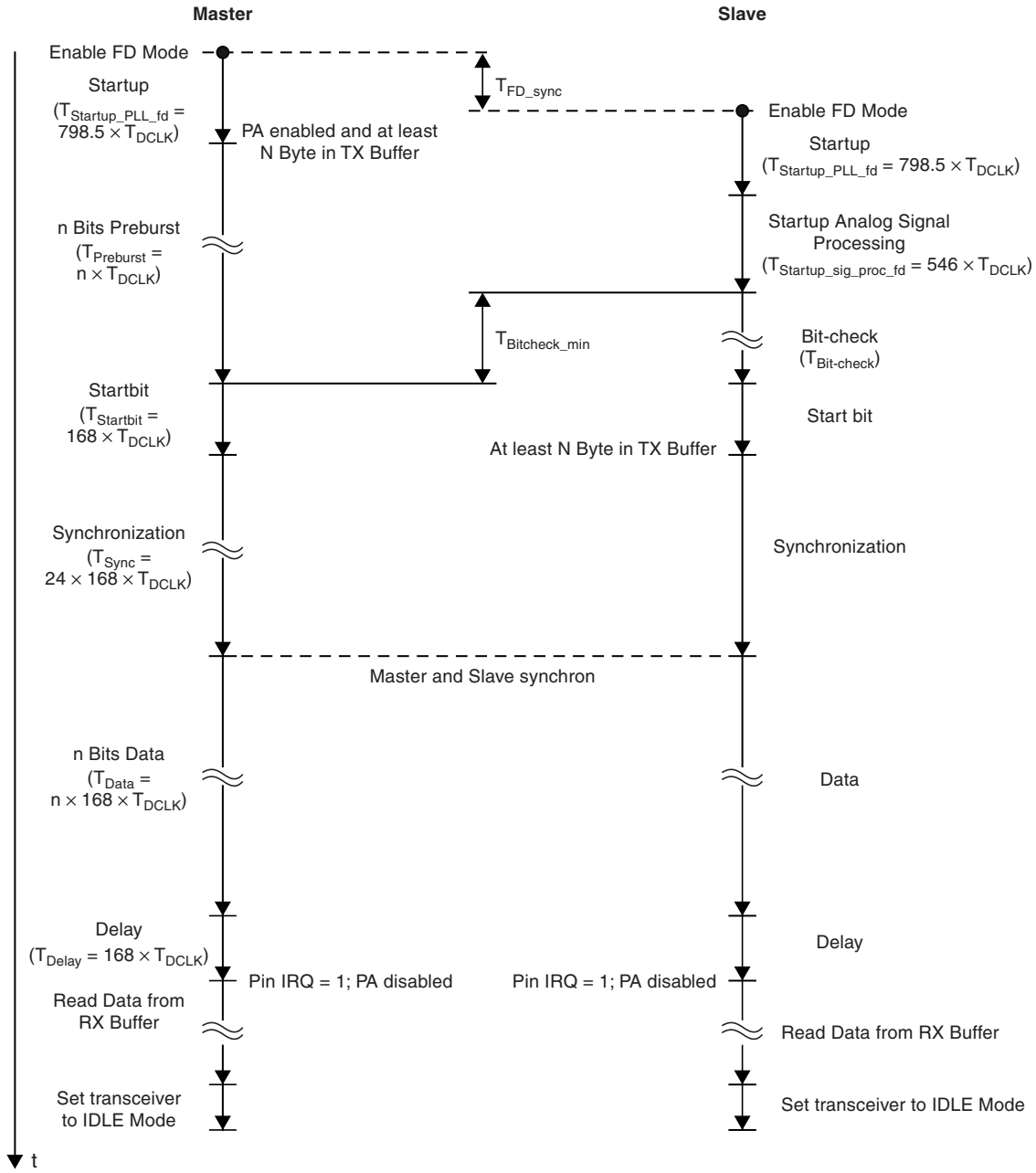


Figure 14-14. Flow FD mode (Master)

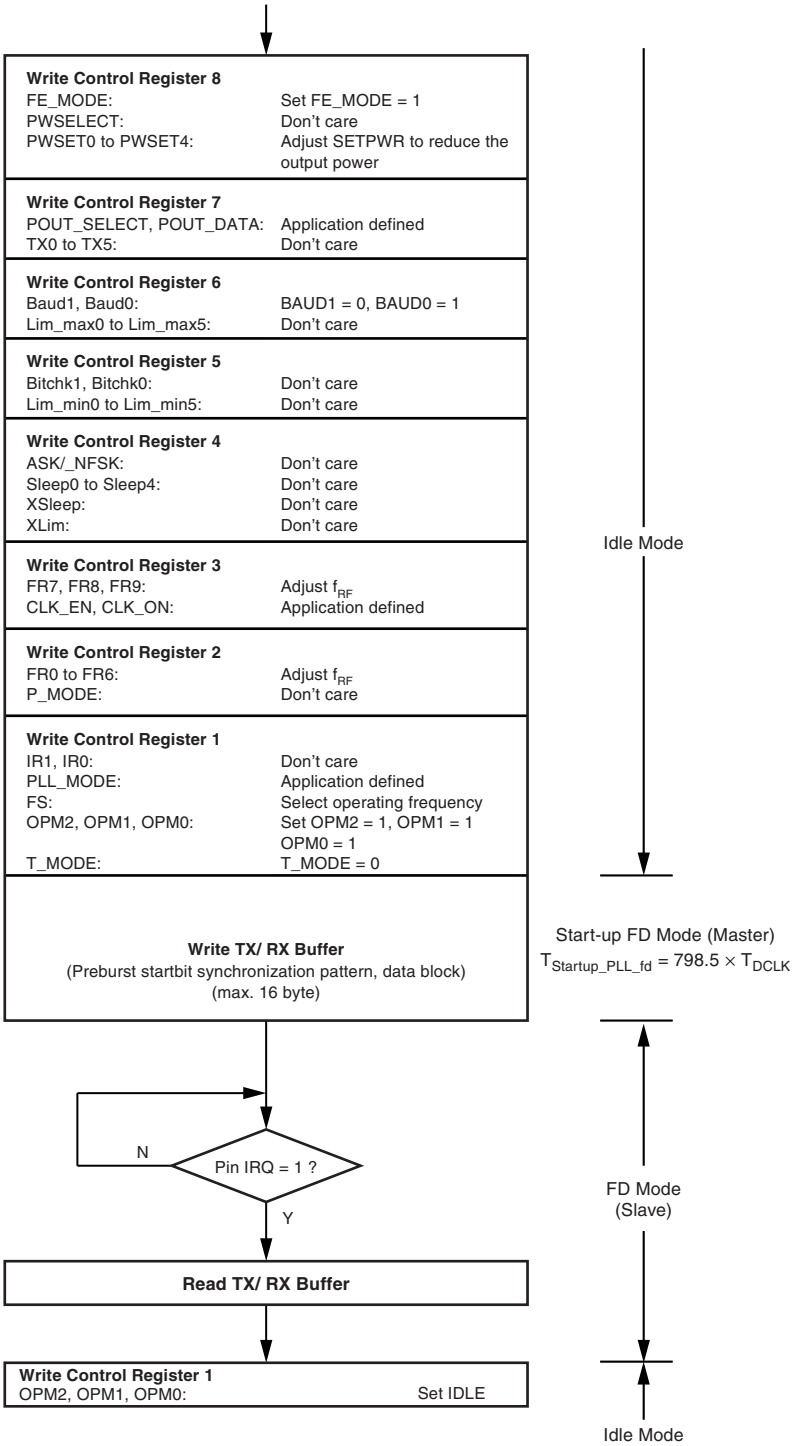
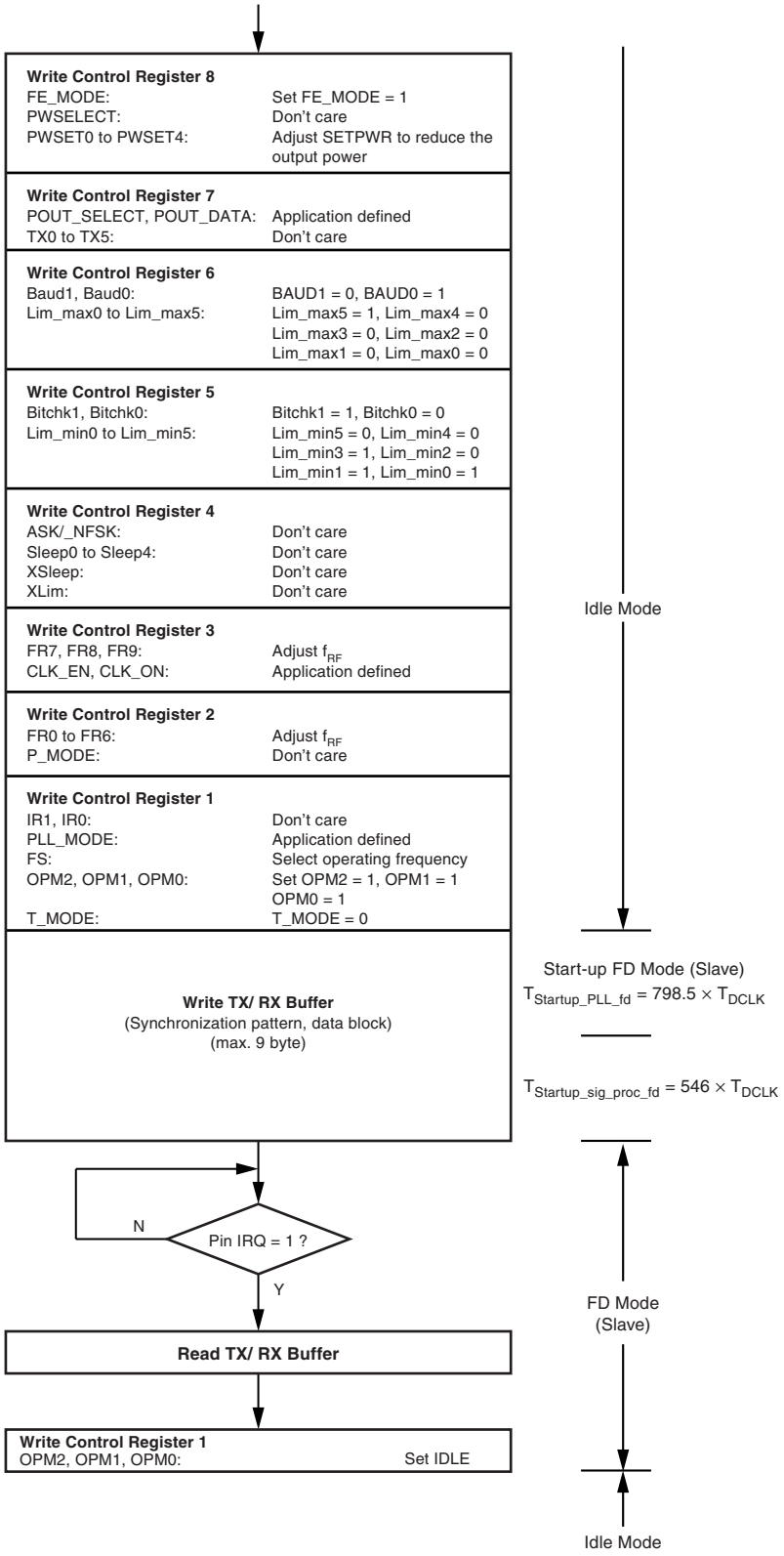


Figure 14-15. Flow FD Mode (Slave)



14.4 Interrupts

Via pin IRQ, the transceiver signals different operating conditions to a connected microcontroller. If a specific operating condition occurs, pin IRQ is set to a high level.

If an interrupt occurs, it is recommended to delete the interrupt immediately by reading the status register, thus the next possible interrupt doesn't get lost. If the Interrupt pin doesn't switch to a low level by reading the status register, the interrupt was triggered by the RX/TX data buffer. In this case, read or write the RX/TX data buffer according to Table 14-8.

Table 14-8. Interrupt Handling

Operating Conditions Which Sets Pin IRQ to High Level	Operations Which Sets Pin IRQ to Low Level
Events in Status Register	
State transition of status bit N_Power_On (0 → 1; 1 → 0)	Read status register or Command delete IRQ
Appearance of status bit Power_On (0 → 1)	
Events During TX Operation (T_MODE = 0)	
1, 2, 4 or 12 bytes are in the TX data buffer or the TX data buffer is empty (depends on IR0 and IR1 in control register 1)	Write TX data buffer or Write control register 1 or Write control register 4 or Write control register 5 or Write control register 6 or Write control register 7 or Command delete IRQ
Events During RX Operation (T_MODE = 0)	
1, 2, 4 or 12 received bytes are in the RX data buffer or a receiving error is occurred (depends on IR0 and IR1 in control register 1)	Read RX data buffer(1) or Write control register 1 or Write control register 4 or Write control register 5 or Write control register 6 or Write control register 7 or Command delete IRQ
Successful Bit-check (P_MODE = 0)	
Events During FD Operation	
TX data buffer empty	Read RX data buffer(1) or Write control register 1 or Write control register 4 or Write control register 5 or Write control register 6 or Write control register 7 or Command delete IRQ

Note: 1. During reading of the RX/TX buffer, no IRQ is issued, due to the received bytes or a receiving error.

15. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	–55	+125	°C
Ambient temperature	T_{amb}	–40	+105	°C
Supply voltage VS2	V_{MaxVS2}	–0.3	+7.2	V
Supply voltage VS1	V_{MaxVS1}	–0.3	+4	V
Supply voltage VSINT	$V_{MaxVSINT}$	–0.3	+5.5	V
ESD (Human Body Model ESD S.5.1) every pin	HBM	–2.5	+2.5	kV
ESD (Machine Model JEDEC A115A) every pin	MM	–200	+200	V
ESD (Field Induced Charge Device Model ESD STM 5.3.1-1999) every pin	FCDM	–500	500	V
Maximum input level, input matched to 50Ω	P_{in_max}		10	dBm

16. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	R_{thJA}	25	K/W

17. Electrical Characteristics: General

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**RX_TX_IDLE Mode**								
1.1	RF operating frequency range	ATA5824 V_{433_N868} = GND	4, 10	f_{RF}	867		870	MHz	A
		ATA5824 V_{433_N868} = AVCC	4, 10	f_{RF}	433		435	MHz	A
		ATA5823 V_{433_N868} = AVCC	4, 10	f_{RF}	314		316	MHz	A
1.2	Supply current OFF mode	$V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V (battery)	17, 18, 27	I_{S_OFF}		< 10		nA	A
		$V_{VS2} = V_{VSINT}$ = 5V (car)	17, 27	I_{S_OFF}		< 10		nA	A
1.3	Supply current IDLE mode	XTO running $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V (battery) CLK disabled	17, 18, 27	I_{S_IDLE}		260		µA	B
		XTO running $V_{VS2} = V_{VSINT}$ = 5V (car) CLK disabled	17, 27	I_{S_IDLE}		350		µA	B
1.4	System start-up time	From OFF mode to IDLE mode including reset and XTO start-up (see Figure 12-4 on page 46) XTAL: C_m = 5 fF, C_0 = 1.8 pF, R_m =15Ω		$T_{PWR_ON_IRQ_1}$		0.3		ms	C
1.5	RX start-up time	From IDLE mode to receiving mode $N_{Bit\text{-}check}$ = 3 Bit rate = 20 Kbit/s, BR_Range_3 (see Figure 14-1 on page 54 and Figure 14-2 on page 55)		$T_{Startup_PLL}$ + $T_{Startup_Sig_Proc}$ + $T_{Bit\text{-}check}$		1.39		ms	A
1.6	TX start-up time	From IDLE mode to TX mode (see Figure 14-10 on page 62)		$T_{Startup}$		0.4		ms	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2	**Receiver/RX Mode**								
2.1	Supply current RX mode	f_{RF} = 433.92 MHz and f_{RF} = 315 MHz	17, 18, 27	I_{S_RX}		10.5		mA	A
		f_{RF} = 868.3 MHz	17, 18, 27	I_{S_RX}		10.3		mA	A
2.2	Supply current RX polling mode	T_{Sleep} = 49.45 ms X_{SLEEP} = 8, Sleep = 5 Bit rate = 20 Kbit/s FSK, CLK disabled	17, 18, 27	I_{S_Poll}		484		µA	C
2.3	Input sensitivity FSK f_{RF} = 433.92 MHz	FSK deviation f_{DEV} = ±19.5 kHz limits according to Table 14-3 on page 60, BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 20 Kbit/s	(4)	S_{REF_FSK}	–103.5	–105.5	–107.0	dBm	B
		Bit rate 2.4 Kbit/s	(4)	S_{REF_FSK}	–107.0	–109.0	–110.5	dBm	B
2.4	Input sensitivity ASK f_{RF} = 433.92 MHz	ASK 100% level of carrier, limits according to Table 14-3 on page 60, BER = 10^{-3} T_{amb} = 25°C							
		Bit rate 10 Kbit/s	(4)	P_{REF_ASK}	–109.5	–111.5	–113.0	dBm	B
		Bit rate 2.4 Kbit/s	(4)	P_{REF_ASK}	–113.5	–115.5	–117.0	dBm	B
2.5	Sensitivity change at f_{RF} = 315 MHz f_{RF} = 868.3 MHz compared to f_{RF} = 433.92 MHz	f_{RF} = 433.92 MHz to f_{RF} = 315 MHz f_{RF} = 433.92 MHz to f_{RF} = 868.3 MHz $S = S_{REF_ASK} + \Delta S_{REF1}$ $S = S_{REF_FSK} + \Delta S_{REF1}$	(4)	ΔS_{REF1}		–1.0 +2.7		dB	B
2.6	Sensitivity change versus temperature, supply voltage and frequency offset	FSK f_{DEV} = ±19.5 kHz $\Delta f_{OFFSET} \leq \pm 75$ kHz ASK 100% $\Delta f_{OFFSET} \leq \pm 75$ kHz $S = S_{REF_ASK} + \Delta S_{REF1} + \Delta S_{REF2}$ $S = S_{REF_FSK} + \Delta S_{REF1} + \Delta S_{REF2}$	(4)	ΔS_{REF2}	+4.5		–1.5		B

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Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.7	RSSI output	Dynamic range	(4), 36	D_{RSSI}		70		dB	A
		Lower level of range f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz	(4), 36	P_{RFIN_Low}		 –116 –115 –112		 dBm dBm dBm	A
		Upper level of range f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz	(4), 36	P_{RFIN_High}		 –46 –45 –42		 dBm dBm dBm	A
		Gain	(4), 36		5.5	8.0	10.5	mV/dB	A
		Output voltage range	(4), 36	OV_{RSSI}	350		1100	mV	A
2.8	Output resistance RSSI pin	RX mode TX mode	36	R_{RSSI}	8 32	10 40	12.5 50	kΩ	C
2.9	Maximum frequency offset in FSK mode	Maximum frequency difference of f_{RF} between receiver and transmitter in FSK mode (f_{RF} is the center frequency of the FSK signal with f_{DEV} = ±19.5 kHz) $P_{RF_IN} \leq$ +10 dBm $P_{RF_IN} \leq P_{RFIN_High}$ (see Figure 7-2 on page 12)	(4)	 $\Delta f_{OFFSET1}$ $\Delta f_{OFFSET2}$	 –69 –75		 +69 +75	kHz	B
2.10	Supported FSK frequency deviation	With up to 2 dB loss of sensitivity. Note that the tolerable frequency offset is for f_{DEV} = ±28 kHz, 8.5 kHz lower than for f_{DEV} = ±19.5 kHz hence $\Delta f_{OFFSET2}$ = ±66.5 kHz	(4)	f_{DEV}	±14	±19.5	±28	kHz	B
2.11	System noise figure	f_{RF} = 315 MHz	(4)	NF		5.5		dB	B
		f_{RF} = 433.92 MHz	(4)	NF		6.5		dB	B
		f_{RF} = 868.3 MHz	(4)	NF		9.7		dB	B
2.12	Intermediate frequency	f_{RF} = 315 MHz		f_{IF}		227		kHz	A
		f_{RF} = 433.92 MHz		f_{IF}		223		kHz	A
		f_{RF} = 868.3 MHz		f_{IF}		226		kHz	A

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Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.13	System bandwidth	**This value is for information only!** Note that for crystal and system frequency offset calculations, Δf_{OFFSET} must be used.	(4)	SBW		220		kHz	A
2.14	System out-band 2nd-order input intercept point with respect to f_{IF}	Δf_{meas1} = 1.800 MHz Δf_{meas2} = 2.026 MHz $f_{IF} = \Delta f_{meas2} - \Delta f_{meas1}$	(4)	IIP2		+50		dBm	C
2.15	System outband 3rd-order input intercept point	Δf_{meas1} = 1.8 MHz Δf_{meas2} = 3.6 MHz f_{RF} = 315 MHz	(4)	IIP3		–22		dBm	C
		f_{RF} = 433.92 MHz	(4)	IIP3		–21		dBm	C
		f_{RF} = 868.3 MHz	(4)	IIP3		–17		dBm	C
2.16	System outband input 1 dB compression point	Δf_{meas1} = 10 MHz f_{RF} = 315 MHz this values are for information only, for blocking behavior see Figure 7-3 on page 15 to Figure 7-7 on page 17	(4)	I1dBCP		–31		dBm	C
		f_{RF} = 433.92 MHz	(4)	I1dBCP		–30		dBm	C
		f_{RF} = 868.3 MHz	(4)	I1dBCP		–27		dBm	C
2.17	LNA input impedance	f_{RF} = 315 MHz	4	Z_{in_LNA}		(44 – j233)		Ω	C
		f_{RF} = 433.92 MHz	4	Z_{in_LNA}		(32 – j169)		Ω	C
		f_{RF} = 868.3 MHz	4	Z_{in_LNA}		(21 – j78)		Ω	C
2.18	Allowable peak RF input level, ASK and FSK	BER < 10^{-3}, ASK: 100%	(4)	P_{IN_max}		+10	–10	dBm	C
		FSK: f_{DEV} = ±19.5 kHz	(4)	P_{IN_max}		+10	–10	dBm	C
2.19	LO spurious at LNA_IN	f < 1 GHz	(4)				–57	dBm	C
		f >1 GHz	(4)				–47	dBm	C
		f_{RF} = 315 MHz	(4)			–100		dBm	C
		f_{RF} = 433.92 MHz	(4)			–98		dBm	C
		f_{RF} = 868.3 MHz	(4)			–85		dBm	C
2.20	Image rejection	Within the complete image band f_{RF} = 315 MHz	(4)		25	30		dB	A
		f_{RF} = 433.92 MHz	(4)		25	30		dB	A
		f_{RF} = 868.3 MHz	(4)		20	25		dB	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
2.21	Useful signal to interferer ratio	Peak level of useful signal to peak level of interferer for BER < 10^{-3} with any modulation scheme of interferer.							
		FSK BR_Ranges 0, 1, 2	(4)	SNR_{FSK0-2}		2	3	dB	B
		FSK BR_Range_3	(4)	SNR_{FSK3}		4	6	dB	B
		ASK ($P_{RF} < P_{RFIN_High}$)	(4)	SNR_{ASK}		10	12	dB	B
2.22	Maximum frequency offset in ASK mode	Maximum frequency difference of f_{RF} between Receiver and transmitter in ASK mode $P_{RF_IN} \leq$+10 dBm $P_{RF_IN} \leq P_{RF_IN_High}$		 $\Delta f_{OFFSET1}$ $\Delta f_{OFFSET2}$	 –79 –85		 +79 +85	kHz	B
2.23	Blocking	According to ETSI regulations, the sensitivity (BER = 10^{-3}) is reduced by 3 dB if a continuous wave blocking signal at ±Δf is ΔP_{Block} higher than the useful signal level (Bit rate = 20 Kbit/s, FSK, f_{DEV} ±19.5 kHz, Manchester code)							
		f_{RF} = 315 MHz Δf ±0.75 MHz Δf ±1.0 MHz Δf ±1.5 MHz Δf ±5.0 MHz Δf ±10.0 MHz Blocking behavior see Figure 7-3 to Figure 7-5 on page 15	(4)	ΔP_{BLOCK}		 55 57 60 66 73		dBC	C
		f_{RF} = 433.92 MHz Δf ±0.75 MHz Δf ±1.0 MHz Δf ±1.5 MHz Δf ±5.0 MHz Δf ±10.0 MHz Blocking behavior see Figure 7-3 to Figure 7-5 on page 15	(4)	ΔP_{BLOCK}		 54 56 59 65 67		dBC	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
		f_{RF} = 868.3 MHz Δf ±0.75 MHz Δf ±1.0 MHz Δf ±1.5 MHz Δf ±5.0 MHz Δf ±10.0 MHz Blocking behavior see Figure 7-3 to Figure 7-5 on page 15	(4)	ΔP_{BLOCK}		49 52 56 64 67		dBC	C
2.24	CDEM	capacitor connected to pin 37 (CDEM)	37		–5%	15	+5%	nF	D
3	**Power Amplifier/TX Mode**								
3.1	Supply current TX mode power amplifier OFF	f_{RF} = 868.3 MHz	17,18, 27	$I_{S_TX_PAOFF}$		6.50		mA	A
		f_{RF} = 433.92 MHz and f_{RF} = 315 MHz	17,18, 27	$I_{S_TX_PAOFF}$		6.95		mA	A
3.2	Output power 1	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = 25°C V_{PWR_H} = GND f_{RF} = 315 MHz R_{R_PWR} = 56 kΩ R_{Lopt} = 2.5 kΩ f_{RF} = 433.92 MHz R_{R_PWR} = 56 kΩ R_{Lopt} = 2.3 kΩ f_{RF} = 868.3 MHz R_{R_PWR} = 30 kΩ R_{Lopt} = 1.3 kΩ RF_OUT matched to R_{Lopt}// j/(2 × π × f_{RF} × 1.0 pF)	(10)	P_{REF1}	–2.5	0	+2.5	dBm	B
3.3	Supply current TX mode power amplifier ON 1 0 dBm	PA on/0 dBm f_{RF} = 315 MHz	17, 18, 27	$I_{S_TX_PAON1}$		8.5		mA	B
		f_{RF} = 433.92 MHz	17, 18, 27	$I_{S_TX_PAON1}$		8.6		mA	B
		f_{RF} = 868.3 MHz	17, 18, 27	$I_{S_TX_PAON1}$		9.6		mA	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.4	Output power 2	$V_{VS1} = V_{VS2}$ = 3 V T_{amb} = 25°C V_{PWR_H} = GND f_{RF} = 315 MHz R_{R_PWR} = 30 kΩ R_{Lopt} = 1.0 kΩ f_{RF} = 433.92 MHz R_{R_PWR} = 27 kΩ R_{Lopt} = 1.1 kΩ f_{RF} = 868.3 MHz R_{R_PWR} = 16 kΩ R_{Lopt} = 0.5 kΩ RF_OUT matched to R_{Lopt}// $j/(2 \times \pi \times f_{RF} \times 1.0\ pF)$	(10)	P_{REF2}	3.5	5.0	6.5	dBm	B
3.5	Supply current TX mode power amplifier ON 2 5 dBm	PA on/5 dBm f_{RF} = 315 MHz	17, 18, 27	$I_{S_TX_PAON2}$		10.3		mA	B
		f_{RF} = 433.92 MHz	17, 18, 27	$I_{S_TX_PAON2}$		10.5		mA	B
		f_{RF} = 868.3 MHz	17, 18, 27	$I_{S_TX_PAON2}$		11.2		mA	B
3.6	Output power 3	$V_{VS1} = V_{VS2}$ = 3 V T_{amb} = 25°C V_{PWR_H} = AVCC f_{RF} = 315 MHz R_{R_PWR} = 30 kΩ R_{Lopt} = 0.38 kΩ f_{RF} = 433.92 MHz R_{R_PWR} = 27 kΩ R_{Lopt} = 0.36 kΩ f_{RF} = 868.3 MHz R_{R_PWR} = 20 kΩ R_{Lopt} = 0.22 kΩ RF_OUT matched to R_{Lopt}// $j/(2 \times \pi \times f_{RF} \times 1.0\ pF)$	(10)	P_{REF3}	8.5	10	11.5	dBm	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
3.7	Supply current TX mode power amplifier ON 3 10 dBm	PA on/10dBm f_{RF} = 315 MHz	17, 18, 27	$I_{S_TX_PAON3}$		15.7		mA	B
		f_{RF} = 433.92 MHz	17, 18, 27	$I_{S_TX_PAON3}$		15.8		mA	B
		f_{RF} = 868.3 MHz	17, 18, 27	$I_{S_TX_PAON3}$		17.3		mA	B
3.8	Output power variation for full temperature and supply voltage range	T_{amb} = –40°C to +105°C $P_{out} = P_{REFX} + \Delta P_{REF}$ x = 1, 2 or 3 $V_{VS1} = V_{VS2}$ = 3.0V	(10)	ΔP_{REF}		–0.8	–1.5	dB	B
		$V_{VS1} = V_{VS2}$ = 2.7V	(10)	ΔP_{REF}			–2.5	dB	B
		$V_{VS1} = V_{VS2}$ = 2.4V	(10)	ΔP_{REF}			–3.5	dB	C
		$V_{VS1} = V_{VS2}$ = 2.15V	(10)	ΔP_{REF}			–4.5	dB	B
3.9	Impedance RF_OUT in RX mode	f_{RF} = 315 MHz	10	$Z_{RF_OUT_RX}$		(36 – j502)		Ω	C
		f_{RF} = 433.92 MHz	10	$Z_{RF_OUT_RX}$		(19 – j366)		Ω	C
		f_{RF} = 868.3 MHz	10	$Z_{RF_OUT_RX}$		(2.8 – j141)		Ω	C
3.10	Noise floor power amplifier	At ±10 MHz/at 5 dBm f_{RF} = 868.3 MHz	(10)	L_{TX10M}		–125		dBC/Hz	C
		f_{RF} = 433.92 MHz	(10)	L_{TX10M}		–126		dBC/Hz	C
		f_{RF} = 315 MHz	(10)	L_{TX10M}		–128		dBC/Hz	C
3.11	ASK modulation rate	This corresponds to 10 Kbit/s Manchester coding and 20 Kbit/s NRZ coding		f_{Data_ASK}	1		10	kHz	C
4	**Full-duplex Mode f_{RF} = 315 MHz and f_{RF} = 433.92 MHz**								
4.1	Supply current FD mode 1	P_{out} = –10 dBm R_{R_PWR} = 22 kΩ PWSET=13 **Load optimized for +5 dBm!**	17,18, 27	I_{S_FD1}		11.9		mA	B
4.2	Supply current FD mode 2	P_{out} = –5 dBm R_{R_PWR} = 22 kΩ PWSET=20 **Load optimized for +5 dBm!**	17,18, 27	I_{S_FD2}		12.5		mA	B
4.3	Supply current FD mode 3	P_{out} = 0 dBm R_{R_PWR} = 22 kΩ PWSET=27 **Load optimized for +5 dBm!**	17,18, 27	I_{S_FD3}		13.7		mA	B

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Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
4.4	Supply current FD mode 4	P_{out} = 5 dBm R_{R_PWR} = 22 kΩ PWSET=31 **Load optimized for +5 dBm!**	17,18, 27	I_{S_FD4}		15.2		mA	B
4.5	Input sensitivity FD mode	$V_{VS1} = V_{VS2}$ = 3 V T_{amb} = 25°C, PER = 5% P(RF_{OUT}@RF_{IN}): –30 dBm –35 dBm –40 dBm –45 dBm –50 dBm Bit rate 5 Kbit/s	(4)	S_{REFRX_FD}	 –88.5 –93.5 –97.5 –100.5 –101.5	 –91 –96 –100 –103 –104	 –92.5 –97.5 –101.5 –104.5 –105.5	dBm	B
4.6	Sensitivity change FD mode	$V_{VS1} = V_{VS2}$ = 2.15V to 3.6V Coupling Phase 0° to 360° T_{amb} = –40°C to +105°C Frequency offset max. ±50 kHz $S = S_{REFRX_FD} + \Delta S_{REFRX_FD}$	(4)	ΔS_{REFRX_FD}	–3	0	5	dB	B
4.7	Output Power FD1	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = 25°C R_{R_PWR} = 22 kΩ PWSET = 13 **Load optimized for +5 dBm!**	(10)	P_{REFTX_FD1}	–12.5	–10	–7.5	dBm	B
4.8	Output Power FD1 variation for full temperature range	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 13 $P = P_{REFTX_FD1} + \Delta P_{REFTX_FD1}$	(10)	ΔP_{REFTX_FD1}	–3	–1.5	2	dB	B
4.9	Output Power FD1 variation for full temperature and supply voltage range	$V_{VS1} = V_{VS2}$ = 2.15V to 3.6V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 13 $P = P_{REFTX_FD1} + \Delta P_{REFTX_FD1}$	(10)	ΔP_{REFTX_FD1}	–5.5		2.5	dB	B
4.10	Output Power FD2	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = 25°C R_{R_PWR} = 22 kΩ PWSET = 20 **Load optimized for +5 dBm!**	(10)	P_{REFTX_FD2}	–7.5	–5	–2.5	dBm	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
4.11	Output Power FD2 variation for full temperature range	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 20 $P = P_{REFTX_FD2} + \Delta P_{REFTX_FD2}$	(10)	ΔP_{REFTX_FD2}	–2.5	–1.2	1	dB	B
4.12	Output Power FD2 variation for full temperature and supply voltage range	$V_{VS1} = V_{VS2}$ = 2.15V to 3.6V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 20 $P = P_{REFTX_FD2} + \Delta P_{REFTX_FD2}$	(10)	ΔP_{REFTX_FD2}	–4.5		1.5	dB	B
4.13	Output Power FD3	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = 25°C R_{R_PWR} = 22 kΩ PWSET = 27 **Load optimized for +5 dBm!**	(10)	P_{REFTX_FD3}	–2.5	0	2.5	dBm	B
4.14	Output Power FD3 variation for full temperature range	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 27 $P = P_{REFTX_FD3} + \Delta P_{REFTX_FD3}$	(10)	ΔP_{REFTX_FD3}	–1.5	–0.8	0.5	dB	B
4.15	Output Power FD3 variation for full temperature and supply voltage range	$V_{VS1} = V_{VS2}$ = 2.15V to 3.6V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 27 $P = P_{REFTX_FD3} + \Delta P_{REFTX_FD3}$	(10)	ΔP_{REFTX_FD3}	–4.5		1	dB	B
4.16	Output Power FD4	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = 25°C R_{R_PWR} = 22 kΩ PWSET = 31 **Load optimized for +5 dBm!**	(10)	P_{REFTX_FD4}	3.5	5	6.5	dBm	B
4.17	Output Power FD4 variation for full temperature range	$V_{VS1} = V_{VS2}$ = 3V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 31 $P = P_{REFTX_FD4} + \Delta P_{REFTX_FD4}$	(10)	ΔP_{REFTX_FD4}	–1.5	–0.8	0.5	dB	B
4.18	Output Power FD4 variation for full temperature and supply voltage range	$V_{VS1} = V_{VS2}$ = 2.15V to 3.6V T_{amb} = –40°C to 105°C R_{R_PWR} = 22 kΩ PWSET = 31 $P = P_{REFTX_FD4} + \Delta P_{REFTX_FD4}$	(10)	ΔP_{REFTX_FD4}	–4.5		1	dB	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
5	**XTO**								
5.1	Pulling XTO due to XTO, C_{L1} and C_{L2} tolerances	Pulling at nominal temperature and supply voltage f_{XTAL} = resonant frequency of the XTAL $C_0 \geq 1.0$ pF $R_m \leq 120\Omega$ $C_m \leq 7.0$ fF $C_m \leq 14$ fF	24, 25	Δf_{XTO1}	–50 –100	f_{XTAL}	+50 +100	ppm	A
5.2	Transconductance XTO at start	At start-up, after start-up the amplitude is regulated to V_{PPXTAL}	24, 25	$g_{m,\ XTO}$		19		ms	B
5.3	XTO start-up time	$C_0 \leq 2.2$ pF $C_m < 14$ fF $R_m \leq 120\Omega$	24, 25	$T_{PWR_ON_IRQ_1}$		300	800	µs	A
5.4	Maximum C_0 of XTAL	Required for stable operation with internal load capacitors	24, 25	C_{0max}			3.8	pF	D
5.5	Internal capacitors	C_{L1} and C_{L2}	24, 25	C_{L1}, C_{L2}	14.8	18 pF	21.2	pF	B
5.6	Pulling of radio frequency f_{RF} due to XTO, C_{L1} and C_{L2} versus temperature and supply changes	1.0 pF $\leq C_0 \leq$ 2.2 pF $C_m = \leq 14$ fF $R_m \leq 120\Omega$ PLL adjusted with FREQ at nominal temperature and supply voltage	4, 10	Δf_{XTO2}	–2		+2	ppm	C
5.7	Amplitude XTAL after start-up	C_m = 5 fF, C_0 = 1.8 pF R_m =15 Ω							
		V(XTAL1, XTAL2) peak-to-peak value	24, 25	V_{PPXTAL}		700		mVpp	C
		V(XTAL1) peak-to-peak value	24	V_{PPXTAL}		350		mVpp	C
5.8	Real part of XTO impedance at start-up	$C_0 \leq 2.2$ pF, small signal start impedance, this value is important for crystal oscillator startup	24, 25	Re_{XTO}		–2000	–1500	Ω	B
5.9	Maximum series resistance R_m of XTAL after start-up	$C_0 \leq 2.2$ pF $C_m \leq 14$ fF	24, 25	R_{m_max}		15	120	Ω	B
5.10	Nominal XTAL load resonant frequency	f_{RF} = 868.3 MHz f_{RF} = 433.92 MHz f_{RF} = 315 MHz	24, 25	f_{XTAL}		13.41191 13.25311 12.73193		MHz MHz MHz	D

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
5.11	External CLK frequency		30	f_{CLK}		$f_{CLK} = \frac{f_{XTO}}{3}$		MHz	D
		f_{RF} = 868.3 MHz CLK division ratio = 3 CLK has nominal 50% duty cycle	30	f_{CLK}		4.471		MHz	D
		f_{RF} = 433.92 MHz CLK division ratio = 3 CLK has nominal 50% duty cycle	30	f_{CLK}		4.418		MHz	D
		f_{RF} = 315 MHz CLK division ratio = 3 CLK has nominal 50% duty cycle	30	f_{CLK}		4.244		MHz	D
5.12	DC voltage after start-up	V_{DC}(XTAL1, XTAL2) XTO running (IDLE mode, RX mode and TX mode)	24, 25	V_{DCXTO}	–150	–30		me	C
6	**Programmable Internal Resistor SETPWR**								
6.1	SETPWR in TX- and FD mode	SETPWR = 800Ω + (31 – PWSET) × 3 kΩ PWSET = 16 (see Table 12-25 on page 43)	19	SETPWR		45.8		kΩ	B
6.2	Tolerance of SETPWR versus temperature and supply voltage range		19	SETPWRTOL	–20% ±500Ω		+20% ±500Ω		B
7	**Synthesizer**								
7.1	Spurious TX mode	At ±f_{CLK}, CLK enabled f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		SP_{TX}		< –75 < –75 –74		dBC	A A B
		At ±f_{XTO} f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		SP_{TX}		–73 –70 –65		dBC	A

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Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
7.2	Spurious RX mode	At $\pm f_{CLK}$, CLK enabled f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		SP_{RX}		 < –75 < –75 < –75		dBC	 A A B
		At $\pm f_{XTO}$ f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		SP_{RX}		 –74 –72 –68		dBC	A
7.3	In loop phase noise TX mode	Measured at 20 kHz distance to carrier f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		L_{TX20k}		 –83 –78 –73		dBC/Hz	A
7.4	Phase noise at 1M RX mode	f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		L_{RX1M}		–121 –120 –113		dBC/Hz	A
7.5	Phase noise at 1M TX mode	f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		L_{TX1M}		–113 –111 –108		dBC/Hz	A
7.6	Phase noise at 10M RX mode	Noise floor		L_{RX10M}		< –132		dBC/Hz	B
7.7	Loop bandwidth PLL TX mode	Frequency where the absolute value loop gain is equal to 1		f_{Loop_PLL}		70		kHz	B
7.8	Frequency deviation TX mode	f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz		f_{DEV_TX}		±18.65 ±19.41 ±19.64		kHz	D
7.9	Frequency resolution	f_{RF} = 315 MHz f_{RF} = 433.92 MHz f_{RF} = 868.3 MHz	4, 10	Δf_{Step_PLL}		777.1 808.9 818.6		Hz	D
7.10	FSK modulation rate	This corresponds to 20 Kbit/s Manchester coding and 40 Kbit/s NRZ coding		f_{Data_FSK}	1		20	kHz	B
8	**RX/TX Switch**								
8.1	Impedance RX mode	RX mode, **pin 38 with short connection to GND**, f_{RF} = 0 Hz (DC)	39	Z_{Switch_RX}		23000		Ω	A
		f_{RF} = 315 MHz	39	Z_{Switch_RX}		(11.3 – j214)		Ω	C
		f_{RF} = 433.92 MHz	39	Z_{Switch_RX}		(10.3 – j153)		Ω	C
		f_{RF} = 868.3 MHz	39	Z_{Switch_RX}		(8.9 – j73)		Ω	C

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Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

17. Electrical Characteristics: General (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V (car application). Typical values are given at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C, f_{RF} = 433.92 MHz (battery application) unless otherwise specified. Details about current consumption, timing and digital pin properties can be found in the specific sections of the “Electrical Characteristics”.

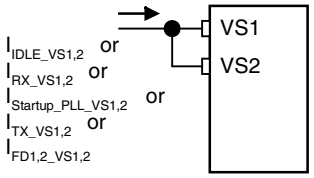
No.	Parameters	Test Conditions	Pin(1)	Symbol	Min.	Typ.	Max.	Unit	Type*
8.2	Impedance TX mode	TX mode, **pin 38 with short connection to GND**, f_{RF} = 0Hz (DC)	39	Z_{Switch_TX}		5		Ω	A
		f_{RF} = 315 MHz	39	Z_{Switch_TX}		(4.8 + j3.2)		Ω	C
		f_{RF} = 433.92 MHz	39	Z_{Switch_TX}		(4.5 + j4.3)		Ω	C
		f_{RF} = 868.3 MHz	39	Z_{Switch_TX}		(5 + j9)		Ω	C
9	**Microcontroller Interface**								
9.1	Voltage range for microcontroller interface		27, 28, 29, 30, 31, 32, 33, 34, 35		2.15		5.25	V	A
9.2	CLK output rise and fall time	f_{CLK} < 4.5 MHz C_L = 10 pF C_L = Load capacitance on pin CLK 2.15V ≤ V_{VSINT} ≤ 5.25V 20% to 80% V_{VSINT}	30	t_{rise} t_{fall}		20 20	30 30	ns ns	B B
9.3	Current consumption of the microcontroller interface	CLK enabled CLK disabled C_L = Load capacitance on pin CLK (All interface pins, except pin CLK, are in stable conditions and unloaded)	27	I_{VSINT}	$I_{VSINT} = \frac{(C_{CLK} + C_L) \times V_{VSINT} \times f_{XTO}}{3}$ < 10 µA				B
9.4	Internal equivalent capacitance	Used for current calculation	30, 27	C_{CLK}		8		pF	B

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Note: 1. Pin numbers in brackets mean they were measured with RF_IN matched to 50Ω according to Figure 7-1 on page 11 with component values according to Table 7-2 on page 12 (RF_{IN}) and RF_OUT matched to 50Ω according to Figure 7-12 on page 22 with component values according to Table 7-7 on page 22 (RF_{OUT}).

18. Electrical Characteristic: Battery Application

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2}$ = 2.15V to 3.6V typical values at $V_{VS1} = V_{VS2}$ = 3V and T_{amb} = 25°C. Application according to Figure 3-1 on page 6 or Figure 5-1 on page 8. f_{RF} = 315.0 MHz/ 433.92 MHz/868.3 MHz unless otherwise specified. Microcontroller interface current I_{VSINT} has to be added.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10	**Battery Application**								
10.1	Supported voltage range (every mode except high power TX mode)	battery application PWR_H = GND	17, 18	V_{VS1}, V_{VS2}	2.15		3.6	V	A
10.2	Supported voltage range (high power TX mode)	battery application PWR_H = AVCC	17, 18	V_{VS1}, V_{VS2}	2.7		3.6	V	A
10.3	Supply voltage for microcontroller interface		27	V_{VSINT}	2.15		5.25	V	A
10.4	Supply current OFF mode	$V_{VS1,2} = V_{VSINT} \leq 3.6V I_{S_OFF} = I_{OFF_VS1,2} + I_{OFF_VSINT}$	17,18, 27	I_{S_OFF}		2	350	nA	A
10.5	Current in IDLE mode on pin VS1 and VS2	$V_{VS1} = V_{VS2} \leq 3V$ CLK enabled CLK disabled	17, 18	$I_{IDLE_VS1,2}$		330 270	570 490	µA µA	A B
10.6	Supply current IDLE mode	CLK enabled	17, 18, 27	I_{S_IDLE}	$I_{S_IDLE} = I_{IDLE_VS1,2} + I_{VSINT}$				
10.7	Current in RX mode on pin VS1and VS2	$V_{VS1} = V_{VS2} \leq 3V$	17, 18	$I_{RX_VS1,2}$		10.5	14	mA	A
10.8	Supply current RX mode	CLK enabled	17, 18, 27	I_{S_RX}	$I_{S_RX} = I_{RX_VS1,2} + I_{VSINT}$				
10.9	Current during $T_{Startup_PLL}$ on pin VS1 and VS2	$V_{VS1} = V_{VS2} \leq 3V$	17, 18	$I_{Startup_PLL_VS1,2}$		8.8	11.5	mA	C
10.10	Current in RX polling mode on pin VS1 and VS2	$I_{Poll} = \frac{I_{IDLE_VS1,2} \times T_{Sleep} + I_{Startup_PLL_VS1,2} \times T_{Startup_PLL} + I_{RX_VS1,2} \times (T_{Startup_Sig_Proc} + T_{Bit\ check})}{T_{Sleep} + T_{Startup_PLL} + T_{Startup_Sig_Proc} + T_{Bitcheck}}$							
10.11	Supply current RX polling mode		17, 18, 27	I_{S_Poll}	$I_{Poll} = I_P + I_{VSINT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

18. Electrical Characteristic: Battery Application (Continued)

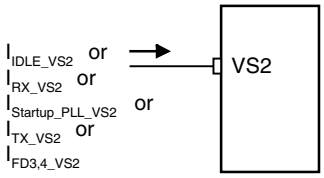
All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, V_{VS1} = V_{VS2} = 2.15V to 3.6V typical values at V_{VS1} = V_{VS2} = 3V and T_{amb} = 25°C. Application according to Figure 3-1 on page 6 or Figure 5-1 on page 8. f_{RF} = 315.0 MHz/ 433.92 MHz/868.3 MHz unless otherwise specified. Microcontroller interface current I_{VSINT} has to be added.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
10.12	Current in TX mode on pin VS1 and VS2	V_{VS1} = V_{VS2} ≤ 3V 315 MHz/5 dBm 315 MHz/10 dBm 433.92 MHz/5 dBm 433.92 MHz/10 dBm 868.3 MHz/5 dBm 868.3 MHz/10 dBm	17, 18	$I_{TX_VS1_VS2}$		 10.3 15.7 10.5 15.8 11.2 17.3	 13.4 20.5 13.5 20.5 14.5 22.5	mA	B
10.13	Supply current TX mode		17, 18, 27	I_{S_TX}	$I_{S_TX} = I_{TX_VS1_VS2} + I_{VSINT}$				
11	**Full-duplex Mode**								
11.1	Current in Full-duplex mode	P_{out} = –10 dBm V_{VS1} = V_{VS2} ≤ 3V R_{R_PWR} = 22 kΩ PWSET = 13 **Load optimized for +5 dBm!**	17, 18, 27	$I_{FD1_VS1_VS2}$		11.9	16.5	mA	B
11.2	Current in Full-duplex mode	P_{out} = –5 dBm V_{VS1} = V_{VS2} ≤ 3V R_{R_PWR} = 22 kΩ PWSET= 20 **Load optimized for +5 dBm!**	17, 18, 27	$I_{FD2_VS1_VS2}$		12.5	17.4	mA	B
11.3	Current in Full-duplex mode	P_{out} = 0 dBm V_{VS1} = V_{VS2} ≤ 3V R_{R_PWR} = 22 kΩ PWSET = 27 **Load optimized for +5 dBm!**	17, 18, 27	$I_{FD3_VS1_VS2}$		13.7	18.3	mA	B
11.4	Supply current Full-duplex mode		17, 18, 27	I_{S_FD}	$I_{S_FD} = I_{FD1,2,3_VS1_VS2} + I_{VSINT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

19. Electrical Characteristics: Car Application

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V. Typical values at V_{VS2} = 5V and T_{amb} = 25°C. Application according to Figure 4-1 on page 7. f_{RF} = 315.0 MHz/433.92 MHz/868.3 MHz unless otherwise specified. Microcontroller interface current I_{VSINT} has to be added.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
12	**Car Application**								
12.1	Supported voltage range	Car application	17	V_{VS2}	4.4		5.6	V	A
12.2	Supply voltage for microcontroller-interface		27	V_{VSINT}	2.15		5.25	V	A
12.3	Supply current OFF mode	$V_{VS2} = V_{VSINT} \leq 5.25V I_{S_OFF} = I_{OFF_VS2} + I_{OFF_VSINT}$	17,27	I_{S_OFF}		0.5	6	µA	A
12.4	Current in IDLE mode on pin VS2	$V_{VS2} \leq 5V$ CLK enabled CLK disabled	17	I_{IDLE_VS2}		430 360	600 520	µA µA	A B
12.5	Supply current IDLE mode	CLK enabled	17, 27	I_{S_IDLE}	$I_{S_IDLE} = I_{IDLE_VS2} + I_{VSINT}$				
12.6	Current in RX mode on pin VS2	V_{VS2} = 5V	17	I_{RX_VS2}		10.8	14.5	mA	B
12.7	Supply current RX mode	CLK enabled	17, 27	I_{S_RX}	$I_{S_RX} = I_{RX_VS2} + I_{VSINT}$				
12.8	Current during $T_{Startup_PLL}$ on pin VS2	V_{VS2} = 5V	17	$I_{Startup_PLL_VS2}$		9.1	12	mA	C
12.9	Current in RX Polling mode on pin VS2	$I_{Poll}'' = \frac{I_{IDLE_VS2} \times T_{Sleep} + I_{Startup_PLL_VS2} \times T_{Startup_PLL} + I_{RX_VS2} \times (T_{Startup_Sig_Proc} + T_{Bit\ check})}{T_{Sleep} + T_{Startup_PLL} + T_{Startup_Sig_Proc} + T_{Bit\ check}}$							
12.10	Supply current RX polling mode		17, 27	I_{S_Poll}	$I_{S_Poll} = I_{Poll} + I_{VSINT}$				
12.11	Current in TX mode on pin VS2	V_{VS2} = 5V 315 MHz/5dBm 315 MHz/10dBm 433.92 MHz/5dBm 433.92 MHz/10dBm 868.3 MHz/5dBm 868.3 MHz/10dBm	17	I_{TX_VS2}		10.7 16.2 10.9 16.3 11.6 17.8	13.9 21.0 14.0 21.0 15.0 23.0	mA	B
12.12	Supply current TX mode		17, 27	I_{S_TX}	$I_{S_TX} = I_{TX_VS2} + I_{VSINT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

19. Electrical Characteristics: Car Application (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C, V_{VS2} = 4.4V to 5.6V, V_{VSINT} = 4.4V to 5.25V. Typical values at V_{VS2} = 5V and T_{amb} = 25°C. Application according to Figure 4-1 on page 7. f_{RF} = 315.0 MHz/433.92 MHz/868.3 MHz unless otherwise specified. Microcontroller interface current I_{VSINT} has to be added.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13	**Full-duplex Mode**								
13.1	Current in Full-duplex mode	P_{out} = –5 dBm V_{VS2} = 5V R_{R_PWR} = 22 kΩ PWSET = 19 **Load optimized for +5 dBm!**	17, 27	I_{FD4_VS2}		12.7	16.9	mA	B
13.2	Current in Full-duplex mode	P_{out} = 0 dBm V_{VS2} = 5V R_{R_PWR} = 22 kΩ PWSET = 26 **Load optimized for +5 dBm!**	17, 27	I_{FD5_VS2}		13.8	18.4	mA	B
13.3	Current in Full-duplex mode	P_{out} = 5 dBm V_{VS2} = 5V R_{R_PWR} = 22 kΩ PWSET = 31 **Load optimized for +5 dBm!**	17, 27	I_{FD6_VS2}		15.6	20.8	mA	B
13.4	Supply current Full-duplex mode		17, 27	I_{S_FD}	$I_{S_FD} = I_{FD4,5,6_VS2} + I_{VSINT}$				

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

20. Digital Timing Characteristics

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C. $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and $V_{VS2} = V_{VSINT}$ = 4.4V to 5.25V (car application), typical values at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
14	**Basic Clock Cycle of the Digital Circuitry**								
14.1	Basic clock cycle			T_{DCLK}	$16/f_{XTO}$		$16/f_{XTO}$	µs	A
14.2	Extended basic clock cycle	XLIM = 0 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3 XLIM = 1 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{XDCLK}	 8 4 2 1 × T_{DCLK} 16 8 4 2 × T_{DCLK}		 8 4 2 1 × T_{DCLK} 16 8 4 2 × T_{DCLK}	µs µs	A A
15	**RX Mode/RX Polling Mode**								
15.1	Sleep time	Sleep and XSleep are defined in control register 4		T_{Sleep}	Sleep × X_{Sleep}× 1024 × T_{DCLK}		Sleep × X_{Sleep}× 1024 × T_{DCLK}	ms	A
15.2	Start-up PLL RX mode	From IDLE mode		$T_{Startup_PLL}$		798.5 × T_{DCLK}	798.5 × T_{DCLK}	µs	A
15.3	Start-up signal processing	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		$T_{Startup_Sig_Proc}$	930 546 354 258 × T_{DCLK}		930 546 354 258 × T_{DCLK}		A
15.4	Time for Bit-check	Average time during polling. No RF signal applied. $f_{Signal} = 1/(2 \times t_{ee})$ Signal data rate Manchester (Lim_min and Lim_max up to ±50% of t_{ee}, see Figure 14-3 on page 55) Bit-check time for a valid input signal f_{Signal} $N_{Bit\text{-}check}$ = 0 $N_{Bit\text{-}check}$ = 3 $N_{Bit\text{-}check}$ = 6 $N_{Bit\text{-}check}$ = 9		T_{Bit_check}	 $3/f_{Signal}$ $6/f_{Signal}$ $9/f_{Signal}$	$1/f_{Signal}$	 $3.5/f_{Signal}$ $6.5/f_{Signal}$ $9.5/f_{Signal}$	ms	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

20. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C. $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and $V_{VS2} = V_{VSINT}$ = 4.4V to 5.25V (car application), typical values at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.5	Bit-rate range	BR_Range = BR_Range0 BR_Range1 BR_Range2 BR_Range3		BR_Range	 1.0 2.0 4.0 8.0		 2.5 5.0 10.0 20.0	Kbit/s	A
15.6	Minimum time period between edges at pin SDO_TMDO in RX transparent mode	XLIM = 0 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3 XLIM = 1 BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3	31	T_{DATA_min}	$10 \times T_{XDCLK}$			µs	A
15.7	Edge-to-edge time period of the data signal for full sensitivity in RX mode	BR_Range_0 BR_Range_1 BR_Range_2 BR_Range_3		T_{DATA}	200 100 50 25		500 250 125 62.5	µs	B
16	**TX Mode**								
16.1	Start-up time	From IDLE mode		$T_{Startup}$		$331.5 \times T_{DCLK}$	$331.5 \times T_{DCLK}$	µs	A
17	**Configuration of the Transceiver with 4-wire Serial Interface**								
17.1	CS set-up time to rising edge of SCK		33, 35	T_{CS_setup}	$1.5 \times T_{DCLK}$			µs	A
17.2	SCK cycle time		33	T_{Cycle}	2			µs	A
17.3	SDI_TMDI set-up time to rising edge of SCK		32, 33	T_{Setup}	250			ns	C
17.4	SDI_TMDI hold time from rising edge of SCK		32, 33	T_{Hold}	250			ns	C
17.5	SDO_TMDO enable time from rising edge of CS		31, 35	T_{Out_enable}			250	ns	C
17.6	SDO_TMDO output delay from falling edge of SCK	C_L = 10 pF	31, 35	T_{Out_delay}			250	ns	C
17.7	SDO_TMDO disable time from falling edge of CS		31, 33	$T_{Out_disable}$			250	ns	C
17.8	CS disable time period		35	$T_{CS_disable}$	$1.5 \times T_{DCLK}$			µs	A
17.9	Time period SCK low to CS high		33, 35	T_{SCK_setup1}	250			ns	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

20. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C. $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and $V_{VS2} = V_{VSINT}$ = 4.4V to 5.25V (car application), typical values at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
17.10	Time period SCK low to CS low		33, 35	T_{SCK_setup2}	250			ns	C
17.11	Time period CS low to SCK high		33, 35	T_{SCK_hold}	250			ns	C
18	**Start Time Push Button N_PWR_ON and PWR_ON** Timing of wake-up via PWR_ON or N_PWR_ON								
18.1	PWR_ON high to positive edge on pin IRQ (Figure 12-4 on page 46)	From OFF mode to IDLE mode, applications according to Figure 3-1 on page 6, Figure 4-1 on page 7, Figure 5-1 on page 8 and Figure 6-1 on page 9 XTAL: C_m < 14 fF (typ. 5 fF) C_0 < 2.2 pF (typ. 1.8 pF) $R_m \leq 120\Omega$ (typ. 15Ω) battery application $C_1 = C_2 = C_3$ = 68 nF $C_5 = C_7$ = 10 nF car application $C_1 = C_3 = C_4$ = 68 nF C_2 = 2.2 µF C_5 = 10 nF	29, 40	$T_{PWR_ON_IRQ_1}$		0.3 0.45	0.8 1.3	ms	B
18.2	PWR_ON high to positive edge on pin IRQ (Figure 12-4 on page 46)	From every mode except OFF mode	29, 40	$T_{PWR_ON_IRQ_2}$			$2 \times T_{DCLK}$	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

20. Digital Timing Characteristics (Continued)

All parameters refer to GND and are valid for T_{amb} = –40°C to +105°C. $V_{VS1} = V_{VS2} = V_{VSINT}$ = 2.15V to 3.6V (battery application), and $V_{VS2} = V_{VSINT}$ = 4.4V to 5.25V (car application), typical values at $V_{VS1} = V_{VS2} = V_{VSINT}$ = 3V and T_{amb} = 25°C unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
18.3	N_PWR_ON low to positive edge on pin IRQ (Figure 12-2 on page 44)	From OFF mode to IDLE mode, applications according to Figure 3-1 on page 6, Figure 4-1 on page 7, Figure 5-1 on page 8 and Figure 6-1 on page 9 XTAL: C_m < 14 fF (typ 5 fF) C_0 < 2.2 pF (typ 1.8 pF) $R_m \leq 120\Omega$ (typ 15Ω) battery application $C_1 = C_2$ = 68 nF $C_3 = C_4$ = 68 nF C_5 = 10 nF car application $C_1 = C_4$ = 68 nF $C_2 = C_3$ = 2.2 µF C_5 = 10 nF	29, 45	$T_{N_PWR_ON_IRQ}$		0.3 0.45	0.8 1.3	ms	B
18.4	Push button debounce time	Every mode except OFF mode	29, 45	$T_{Debounce}$	8195 × T_{DCLK}		8195 × T_{DCLK}	µs	A
19	**Full-duplex Mode**								
19.1	Start-up PLL in Full-duplex mode	From IDLE mode		$T_{Startup_PLL_fd}$	798.5 × T_{DCLK}		798.5 × T_{DCLK}	µs	A
19.2	Start-up signal processing FD mode	Data rate is fixed for full-duplex operation		$T_{Startup_Sig_Proc_fd}$	546 × T_{DCLK}		546 × T_{DCLK}	µs	A
19.3	Time per information Bit in Full-duplex mode	Data rate is fixed for full-duplex operation		T_{BIT_fd}	168 × T_{DCLK}		168 × T_{DCLK}	µs	A
19.4	Switch OFF Delay	Time from last transmitted bit to switch of the power amplifier		T_{Delay}	168 × T_{DCLK}		168 × T_{DCLK}	µs	A
19.5	Synchronization Time	Time after startbit detection to begin of payload data transmission		T_{Sync}	24 × T_{BIT-fd}		24 × T_{BIT-fd}	µs	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

21. Digital Port Characteristics

All parameter refer to GND and valid for T_{amb} = –40°C to +105°C, V_{VS1} = V_{VS2} = 2.15V to 3.6V (battery application) and V_{VS2} = 4.4V to 5.25V (car application) typical values at V_{VS1} = V_{VS2} = 3V (battery application) and T_{amb} = 25°C unless otherwise specified.
V_{VSINT} = 2.15V to 5.25V can be used independent from V_{VS1} and V_{VS2} in the case the microcontroller uses an different supply voltage.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
20	**Digital Ports**								
20.1	CS input - low level input voltage	V_{VSINT} = 2.15V to 5.25V	35	V_{Il}			0.2 × V_{VSINT}	V	A
	- high level input voltage	V_{VSINT} = 2.15V to 5.25V	35	V_{Ih}	0.8 × V_{VSINT}			V	A
20.2	SCK input - low level input voltage	V_{VSINT} = 2.15V to 5.25V	33	V_{Il}			0.2 × V_{VSINT}	V	A
	- high level input voltage	V_{VSINT} = 2.15V to 5.25V	33	V_{Ih}	0.8 × V_{VSINT}			V	A
20.3	SDI_TMDI input - low level input voltage	V_{VSINT} = 2.15V to 5.25V	32	V_{Il}			0.2 × V_{VSINT}	V	A
	- high level input voltage	V_{VSINT} = 2.15V to 5.25V	32	V_{Ih}	0.8 × V_{VSINT}			V	A
20.4	TEST1 input	TEST1 input must always be directly connected to GND	20		0		0	V	
20.5	TEST2 input	TEST2 input must always be direct connected to GND	23		0		0	V	
20.6	PWR_ON input - low level input voltage	V_{VSINT} = 2.15V to 5.25V	40	V_{Il}			0.2 × V_{VSINT}	V	A
	- high level input voltage	V_{VSINT} = 2.15V to 5.25V	40	V_{Ih}	0.8 × V_{VSINT}			V	A
20.7	N_PWR_ON input - low level input voltage	V_{VSINT} = 2.15V to 5.25V Internal pull-up resistor of 50 kΩ ±20%	45	V_{Il}			0.2 × V_{VSINT}	V	A
	- high level input voltage	V_{VSINT} = 2.15V to 5.25V Internal pull-up resistor of 50 kΩ ±20%	45	V_{Ih}	0.8 × V_{VSINT}			V	A
20.8	CS_POL input -low level input voltage		22	V_{Il}			0.2 × V_{DVCC}	V	A
	- high level input voltage		22	V_{Ih}	0.8 × V_{DVCC}		V_{DVCC}	V	A
20.9	SCK_POL input - low level input voltage		43	V_{Il}			0.2 × V_{DVCC}	V	A
	- high level input voltage		43	V_{Ih}	0.8 × V_{DVCC}		V_{DVCC}	V	A
20.10	SCK_PHA input - low level input voltage		44	V_{Il}			0.2 × V_{DVCC}	V	A
	- high level input voltage		44	V_{Ih}	0.8 × V_{DVCC}		V_{DVCC}	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

21. Digital Port Characteristics (Continued)

All parameter refer to GND and valid for T_{amb} = –40°C to +105°C, $V_{VS1} = V_{VS2}$ = 2.15V to 3.6V (battery application) and V_{VS2} = 4.4V to 5.25V (car application) typical values at $V_{VS1} = V_{VS2}$ = 3V (battery application) and T_{amb} = 25°C unless otherwise specified.
V_{VSINT} = 2.15V to 5.25V can be used independent from V_{VS1} and V_{VS2} in the case the microcontroller uses an different supply voltage.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
20.11	433_N868 input - low level input voltage		6	V_{Il}			0.25	V	A
	- high level input voltage		6	V_{Ih}	1.7		AVCC	V	A
20.12	PWR_H input - low level input voltage		9	V_{Il}			0.25	V	A
	- high level input voltage		9	V_{Ih}	1.7		AVCC	V	A
20.13	SDO_TMDO output - saturation voltage low	V_{VSINT} = 2.15V to 5.25V I_{SDO_TMDO} = 250 µA	31	V_{ol}		0.15	0.4	V	B
	- saturation voltage high	V_{VSINT} = 2.15V to 5.25V I_{SDO_TMDO} = –250 µA	31	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
20.14	IRQ output - saturation voltage low	V_{VSINT} = 2.15V to 5.25V I_{IRQ} = 250 µA	29	V_{ol}		0.15	0.4	V	B
	- saturation voltage high	V_{VSINT} = 2.15V to 5.25V I_{IRQ} = –250 µA	29	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
20.15	CLK output - saturation voltage low	V_{VSINT} = 2.15V to 5.25V I_{CLK} = 100 µA internal series resistor of 1 kΩ for spurious reduction in PLL	30	V_{ol}		0.15	0.4	V	B
	- saturation voltage high	V_{VSINT} = 2.15V to 5.25V I_{CLK} = –100 µA internal series resistor of 1 kΩ for spurious reduction in PLL	30	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
20.16	POUT output - saturation voltage low	V_{VSINT} = 2.15V to 5.25V I_{POUT} = 250 µA	28	V_{ol}		0.15	0.4	V	B
	POUT output - saturation voltage low	V_{VSINT} = 5V I_{POUT} = 1000 µA	28	V_{ol}		0.4	0.6	V	B
	POUT output - saturation voltage high	V_{VSINT} = 2.15V to 5.25V I_{POUT} = –1500 µA	28	V_{oh}	V_{VSINT} – 0.4	V_{VSINT} – 0.15		V	B
20.17	RX_ACTIVE output - saturation voltage low	I_{RX_ACTIVE} = 25 µA	46	V_{ol}		0.25	0.4	V	B
	RX_ACTIVE output - saturation voltage high	I_{RX_ACTIVE} = –1500 µA	46	V_{oh}	V_{AVCC} – 0.5	V_{AVCC} – 0.15		V	B
20.18	TEST3 output	TEST3 output must always be directly connected to GND	34		0		0	V	

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

22. Ordering Information

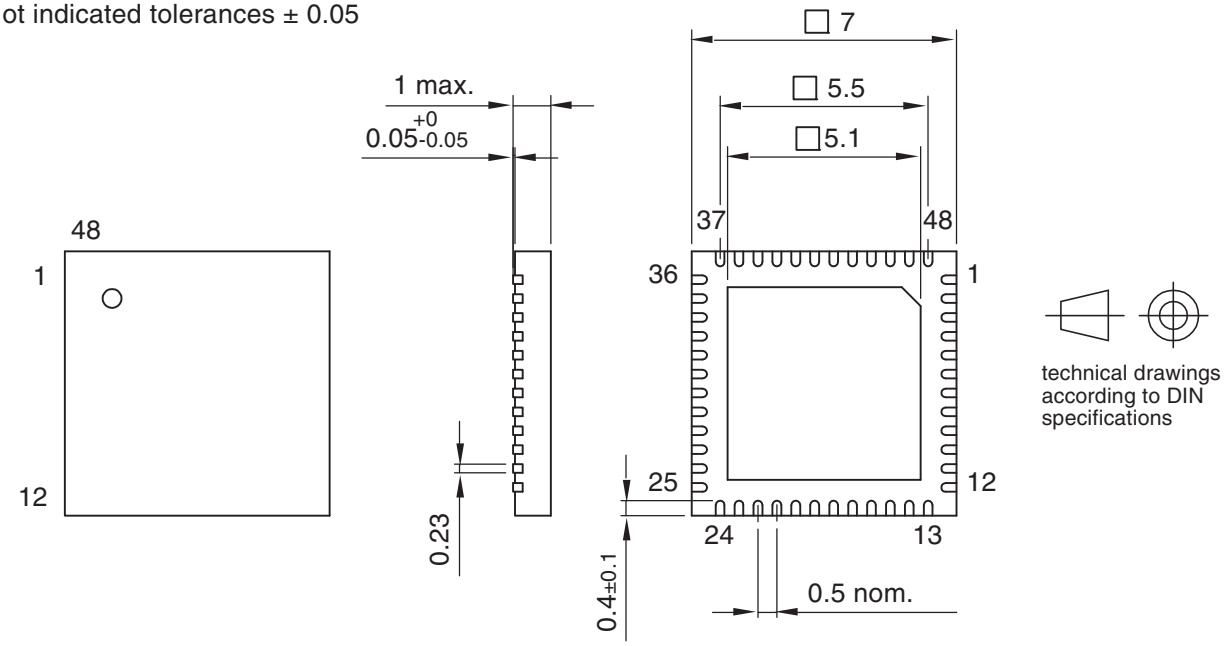
Extended Type Number	Package	Remarks
ATA5823-PLQW	QFN48	7 mm x 7 mm, Pb-free
ATA5824-PLQW	QFN48	7 mm x 7 mm, Pb-free

23. Package Information

Package: QFN 48 - 7 x 7
Exposed pad 5.1 x 5.1

Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5089.02-4

Issue: 1; 14.01.03

24. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4829D-RKE-06/06	• Put datasheet in a new template • kBaud replaced through Kbit/s • Baud replaced through bit • Table 14-8 “Interrupt Handling” on page 70 changed

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